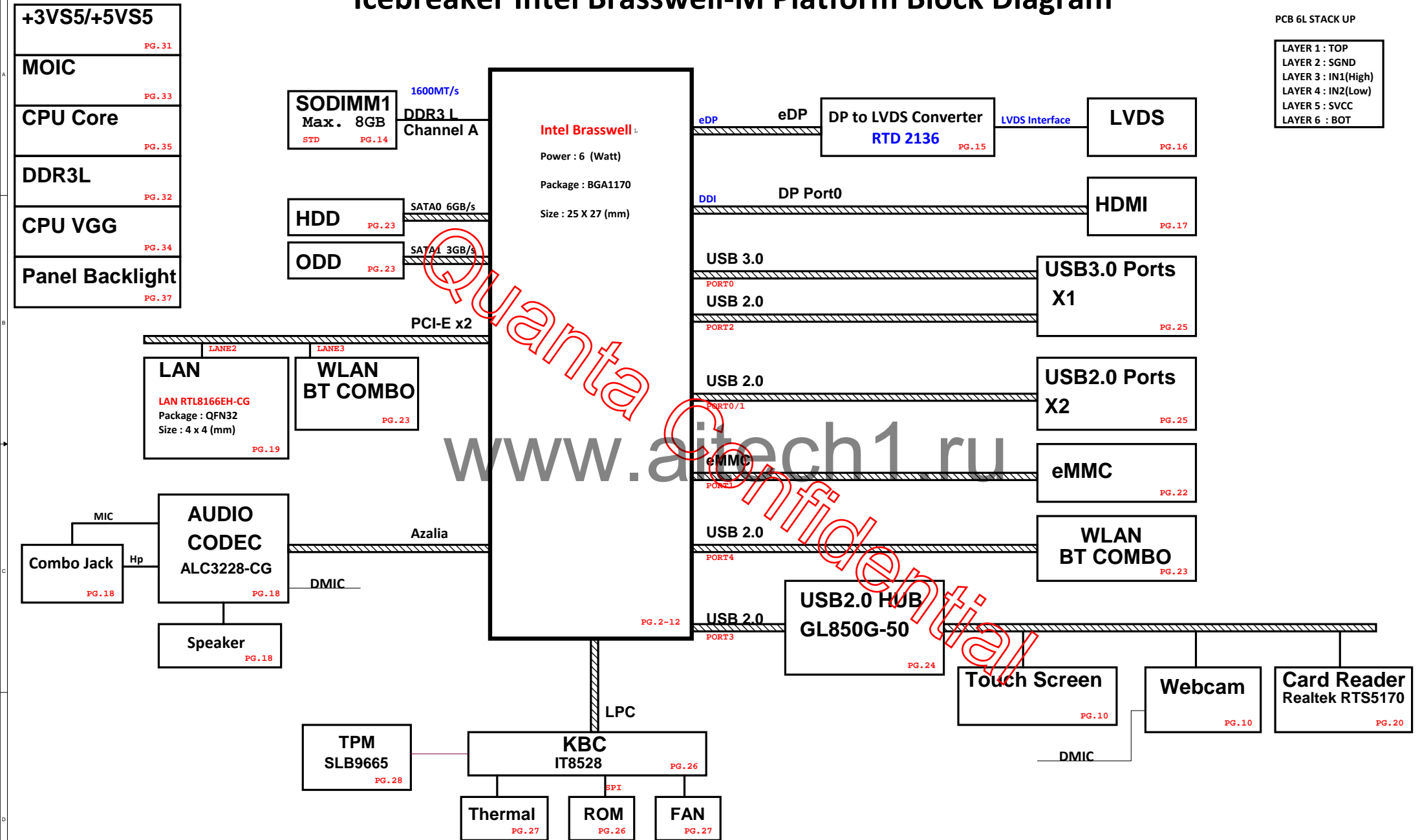


# Icebreaker Intel Brasswell-M Platform Block Diagram

PCB 6L STACK UP

LAYER 1 : TOP  
LAYER 2 : SGND  
LAYER 3 : IN1(High)  
LAYER 4 : IN2(Low)  
LAYER 5 : SVCC  
LAYER 6 : BOT

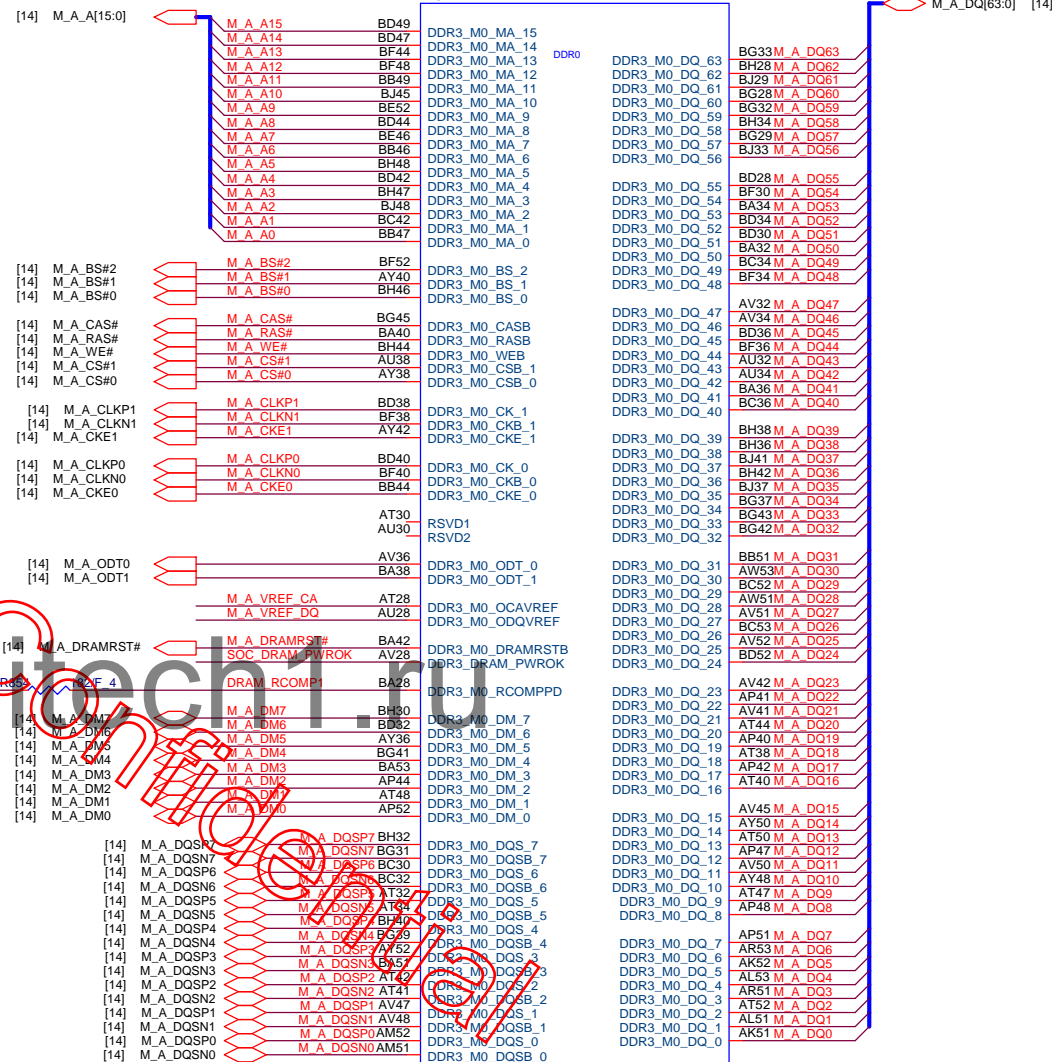


Channel 0 need to  
be populated first for the platform to power on

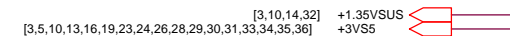
PLACE TWO 4.7K RESISTORS CLOSE TO CPU PINS ON M\_VREF  
ROUTE THE VREF POWER SIGNALS WITH THICK TRACES

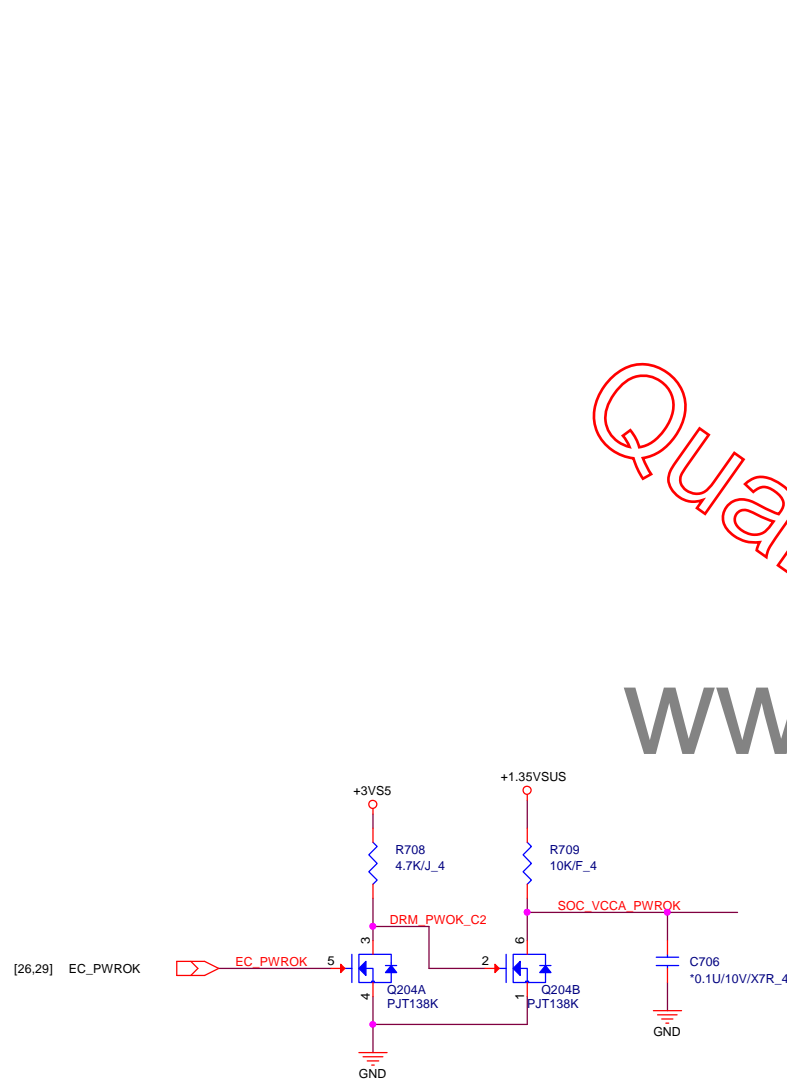


Quanta



BSW\_MCP\_EDS 1 OF 13



TP740  
TP738M\_B\_VREF\_CA  
M\_B\_VREF\_DQ

SOC\_VCCA\_PWROK

GND

U711B BSW\_MCP\_EDS

DDR1_A	
BD5	DDR3_M1_MA_15
BD7	DDR3_M1_MA_14
BF10	DDR3_M1_MA_13
BF6	DDR3_M1_MA_12
BB5	DDR3_M1_MA_11
BJ9	DDR3_M1_MA_10
BE2	DDR3_M1_MA_9
BD10	DDR3_M1_MA_8
BE8	DDR3_M1_MA_7
BB8	DDR3_M1_MA_6
BH6	DDR3_M1_MA_5
BD12	DDR3_M1_MA_4
BH7	DDR3_M1_MA_3
BJ6	DDR3_M1_MA_2
BC12	DDR3_M1_MA_1
BB7	DDR3_M1_MA_0
BF2	DDR3_M1_BS_2
AY14	DDR3_M1_BS_1
BH8	DDR3_M1_BS_0
BG9	DDR3_M1_CASB
BA14	DDR3_M1_RASB
BH10	DDR3_M1_WEB
AU16	DDR3_M1_CSB_1
AY16	DDR3_M1_CSB_0
BD16	DDR3_M1_CK_1
BF16	DDR3_M1_CKB_1
AY12	DDR3_M1_CKE_1
BD14	DDR3_M1_CK_0
BF14	DDR3_M1_CKB_0
BB10	DDR3_M1_CKE_0
AT24	RSVD1
AU24	RSVD2
AV18	DDR3_M1_ODT_0
BA16	DDR3_M1_ODT_1
AT26	DDR3_M1_OCAVREF
AU26	DDR3_M1_ODQVREF
BA12	DDR3_M1_DRAMRSTB
AV26	DDR3_M1_VCCA_PWROK
BA26	DDR3_M1_RCOMP
BH24	DDR3_M1_DM_7
BD22	DDR3_M1_DM_6
AV18	DDR3_M1_DM_5
BG13	DDR3_M1_DM_4
BA1	DDR3_M1_DM_3
AP10	DDR3_M1_DM_2
AT6	DDR3_M1_DM_1
AP2	DDR3_M1_DM_0
BH22	DDR3_M1_DQS_7
BG23	DDR3_M1_DQS_6
BC24	DDR3_M1_DQS_5
AT22	DDR3_M1_DQS_4
BD20	DDR3_M1_DQS_3
BH14	DDR3_M1_DQS_2
BG15	DDR3_M1_DQS_1
AY2	DDR3_M1_DQS_0
BA3	DDR3_M1_DQSB_7
AT12	DDR3_M1_DQSB_6
AT13	DDR3_M1_DQSB_5
AV7	DDR3_M1_DQSB_4
AV6	DDR3_M1_DQSB_3
AM2	DDR3_M1_DQSB_2
AM3	DDR3_M1_DQSB_1
	DDR3_M1_DQSB_0
	DDR3_M1_DQ_63
	DDR3_M1_DQ_62
	DDR3_M1_DQ_61
	DDR3_M1_DQ_60
	DDR3_M1_DQ_59
	DDR3_M1_DQ_58
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	DDR3_M1_DQ_7
	DDR3_M1_DQ_6
	DDR3_M1_DQ_5
	DDR3_M1_DQ_4
	DDR3_M1_DQ_3
	DDR3_M1_DQ_2
	DDR3_M1_DQ_1
	DDR3_M1_DQ_0

BSW\_MCP\_EDS

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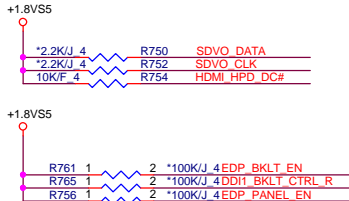
[2,10,14,32] +1.35VSUS  
[2,5,10,13,16,19,23,24,26,28,29,30,31,33,34,35,36] +3VS5



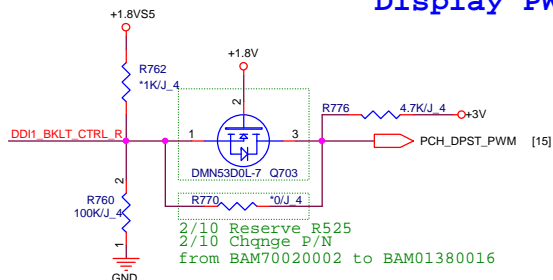
PROJECT N69A

Quanta Computer Inc.

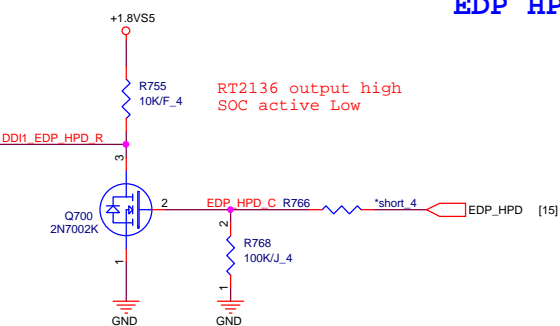
Size Document Number Valley 2/9 (DDR8) Rev 1A  
Date: Thursday, July 23, 2015 Sheet 3 of 43



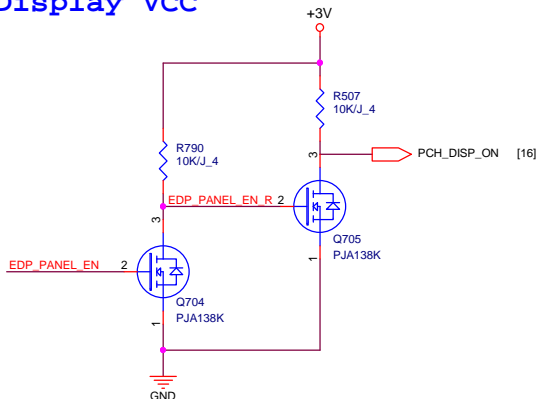
## Display PWM



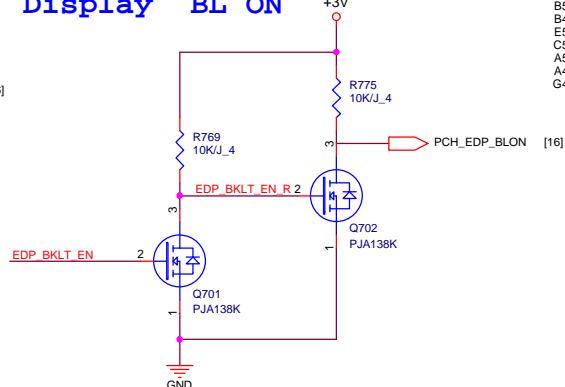
## EDP HPD



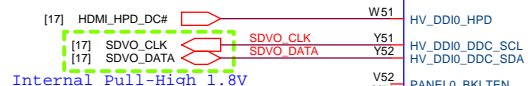
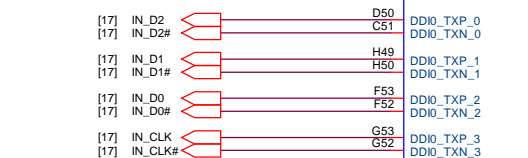
## Display VCC



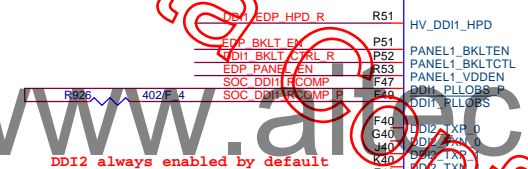
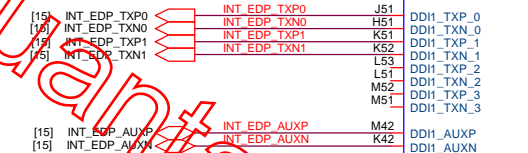
## Display BL ON



## HDMI



## LVDS



U711C

BSW\_MCP\_EDS

DDIO

DD11

NC's

BSW\_MCP\_EDS

MCSI and Camera Interface

MCSI\_COMP

SDMMC1\_CLK

SDMMC1\_CMD

SDMMC1\_D0

SDMMC1\_D1

SDMMC1\_D2

SDMMC1\_D3\_CD\_B

MMC1\_D4\_SD\_WE

MMC1\_D5

MMC1\_D6

MMC1\_D7

MMC1\_RCLK

SDMMC1\_RCOMP

SDMMC2\_CLK

SDMMC2\_CMD

SDMMC2\_D0

SDMMC2\_D1

SDMMC2\_D2

SDMMC2\_D3\_CD\_B

SDMMC3\_CLK

SDMMC3\_CMD

SDMMC3\_D0

SDMMC3\_D1

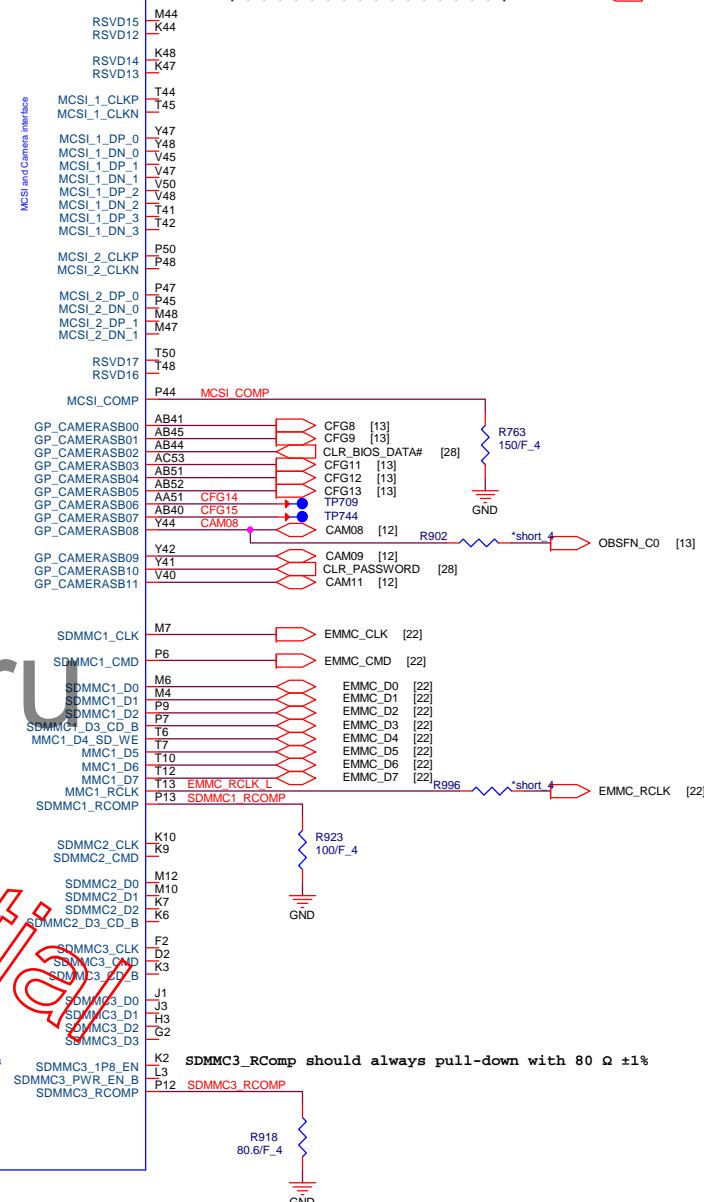
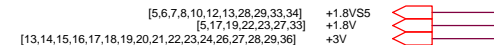
SDMMC3\_D2

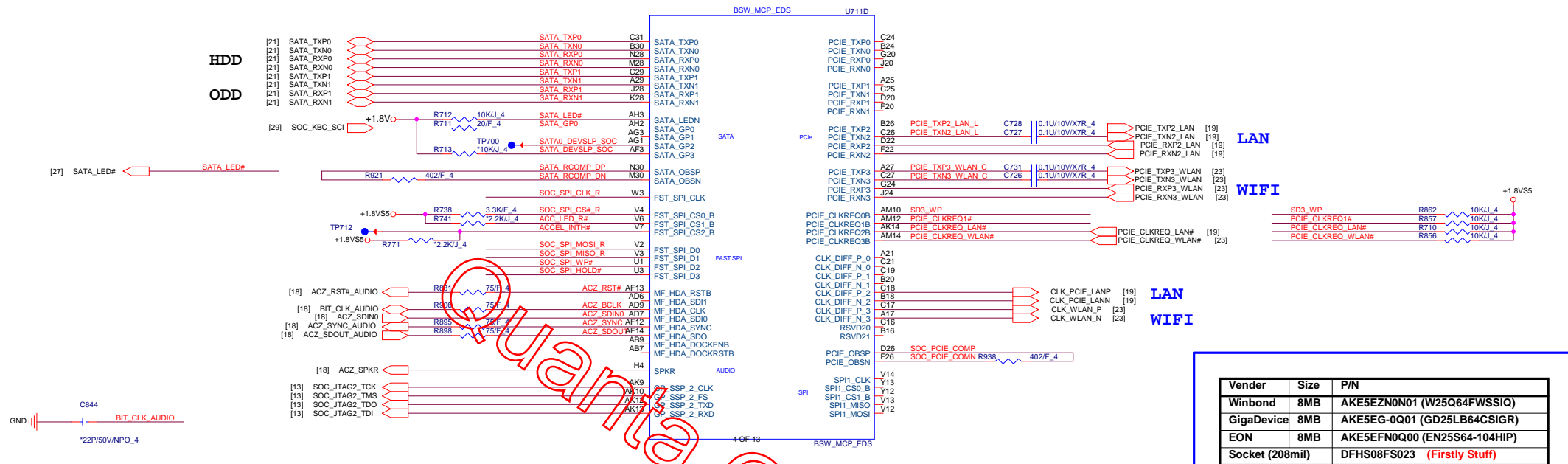
SDMMC3\_D3

SDMMC3\_1P8

SDMMC3\_PWR\_EN\_B

SDMMC3\_RCOMP





To ROM recovery

ROM recovery (for pre-production only)

SPI ROM Socket

U700

SOC\_SPI\_CS# R2 1 VDD 8 SPI\_VCC

SOC\_SPI\_CLK R2 6 SCK 6

SOC\_SPI\_MISO R2 5 SI 7 SPI\_7P

SOC\_SPI\_MISO R2 2 SO HOLD# 4

SPI\_3P 3 WP# VSS 4

\*A25LQ32AM-F/Q

DFHS08FS023

91960-0084L-8P-SOCKET

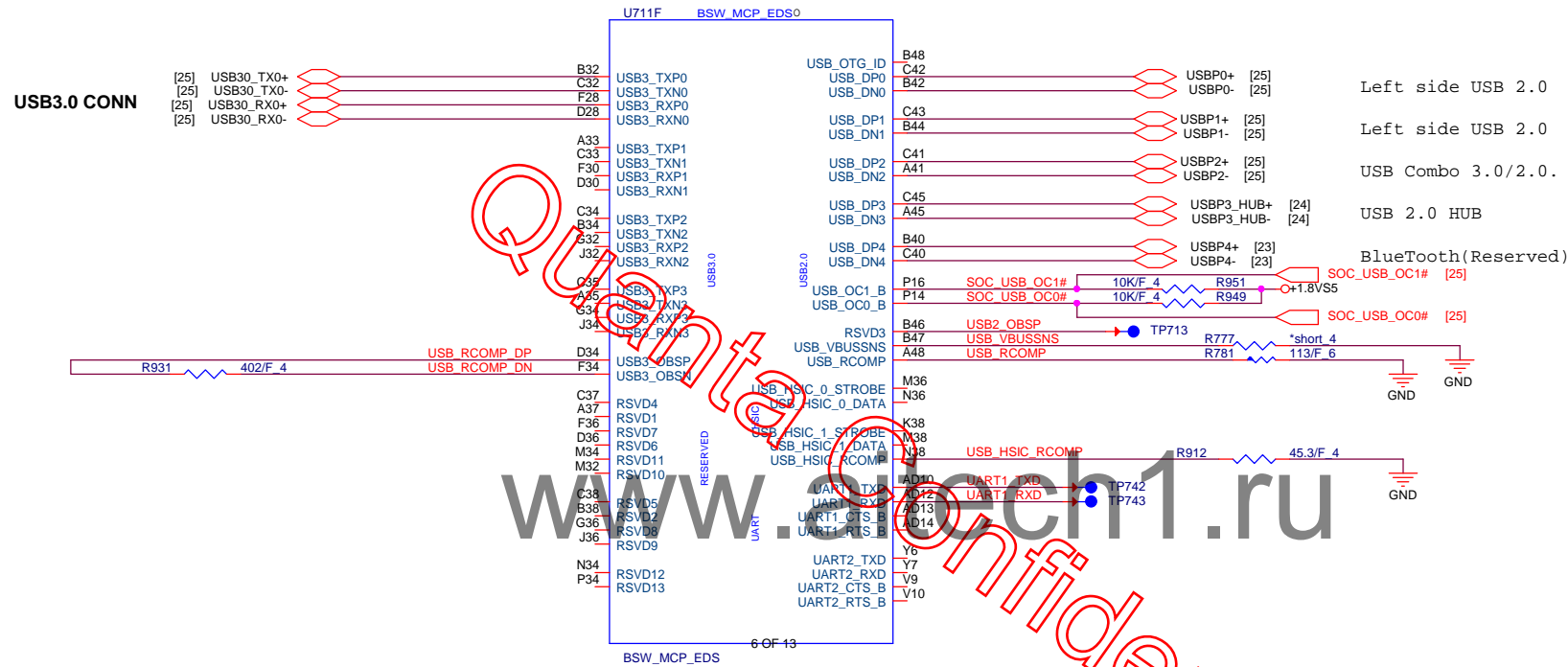
U21 &amp; U22 footprint 要重疊

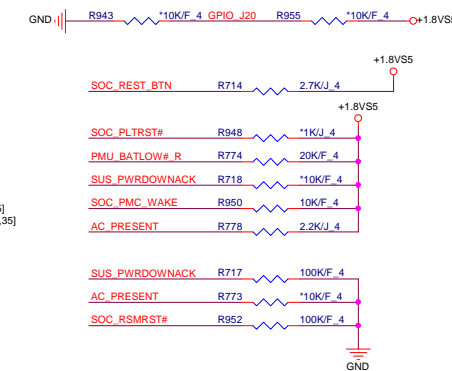
For EMI

\*10P/50V/COG 4 | C738 SOC\_SPI\_CLK\_R2

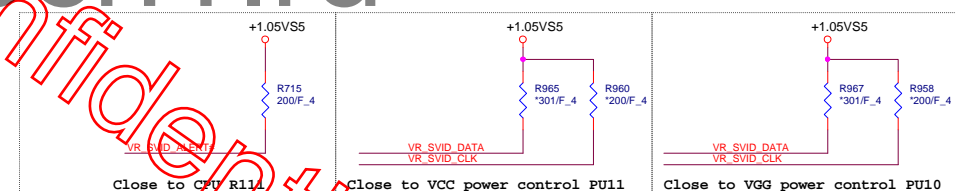


The diagram shows the internal circuitry of the EC-MV-02 module. It features 16 pins connected to a common ground (GND) and a +1.8VSS supply. The resistors are arranged in two columns of eight. The left column resistors are labeled BOARD\_ID0 through BOARD\_ID7, and the right column resistors are labeled BOARD\_ID0 through BOARD\_ID7. The resistors are connected to a common ground (GND) and a +1.8VSS supply. The module is labeled EC-MV-02.



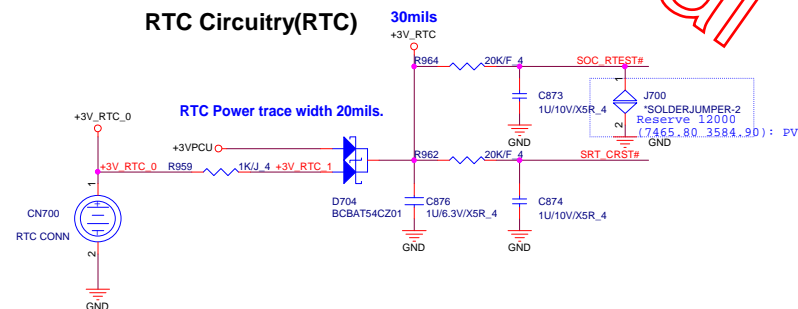


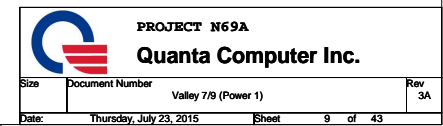
www.aitech1.ru

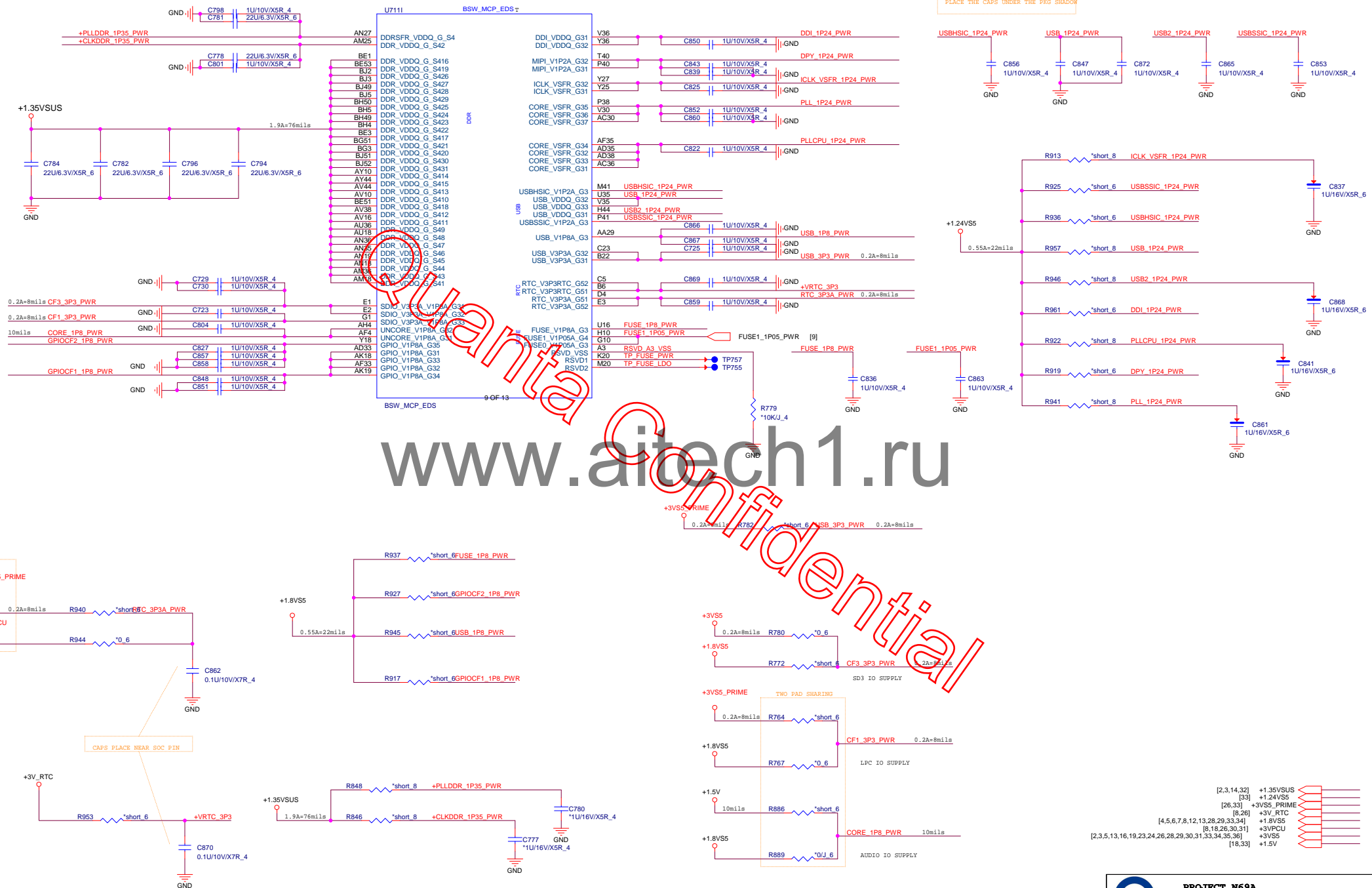


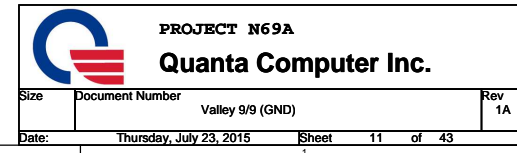
30mils

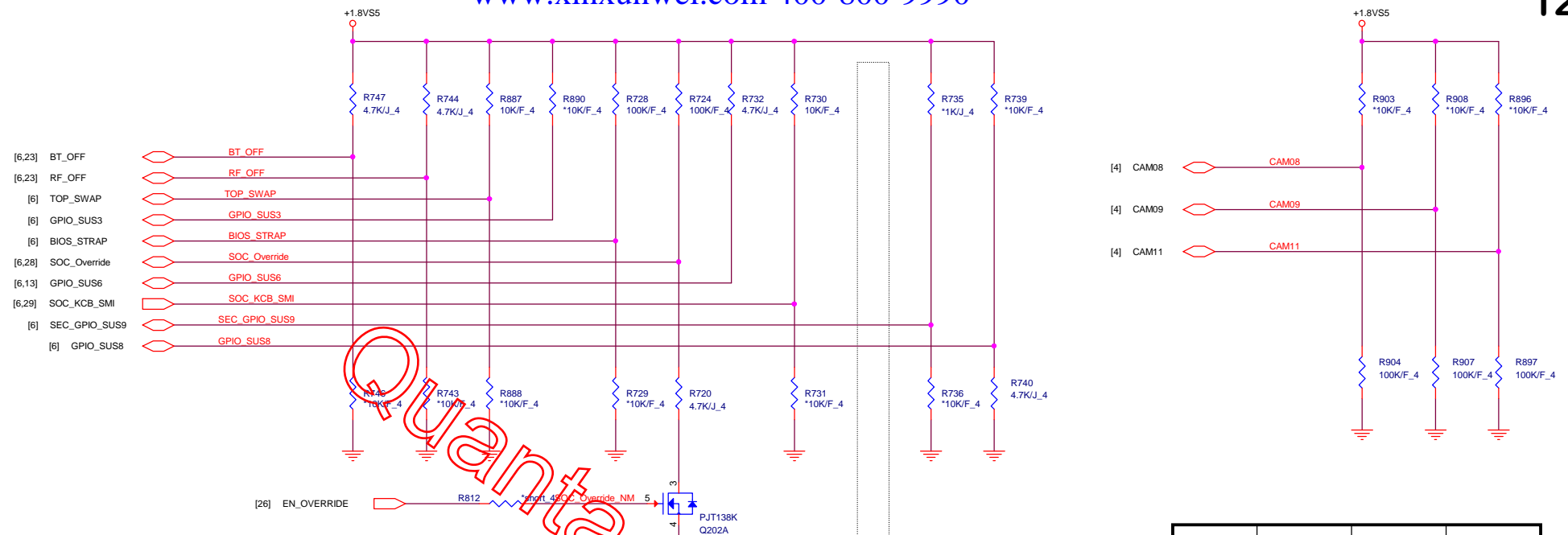
RTC Power trace width 20mils.











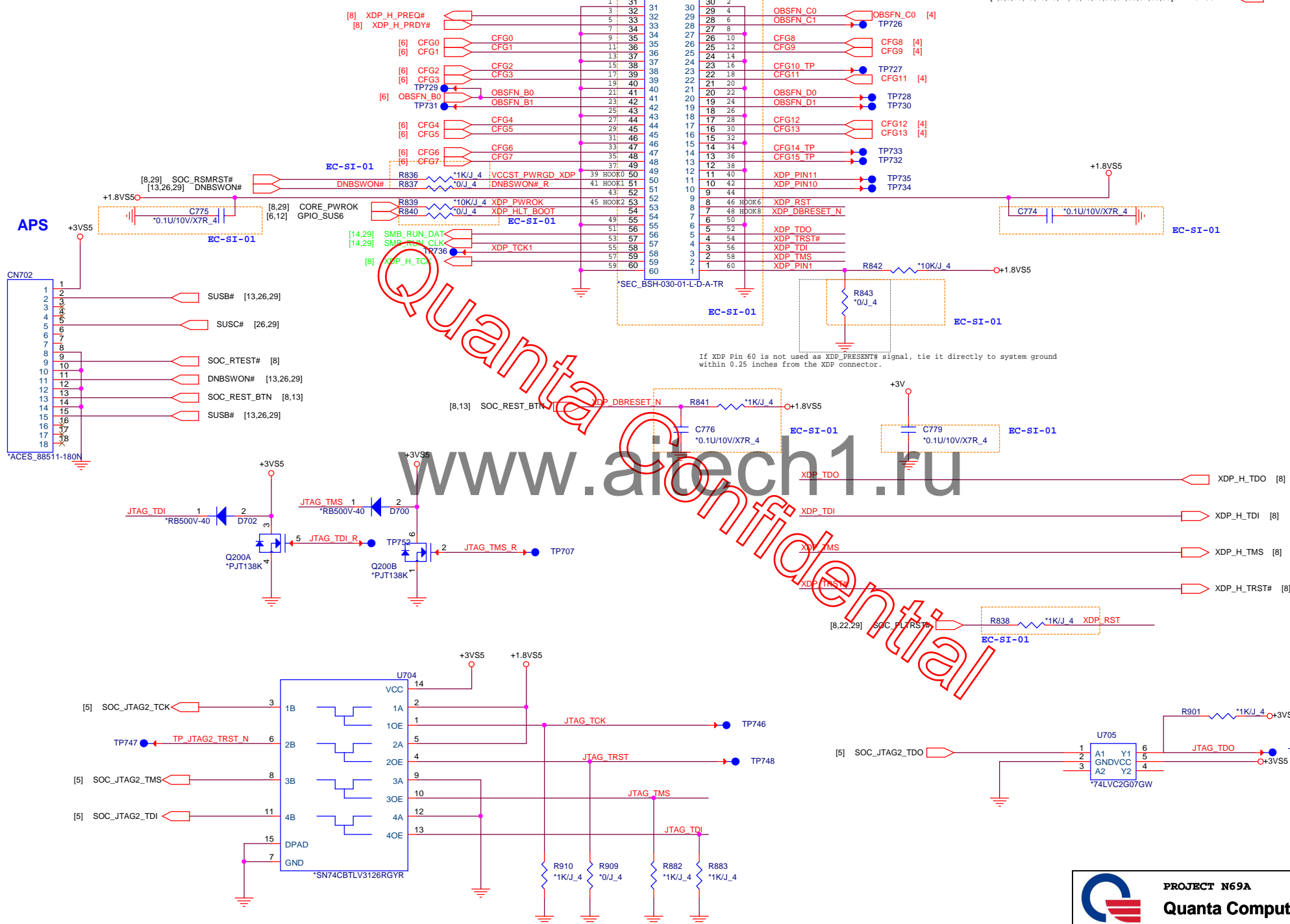
20141112:  
Del unused R

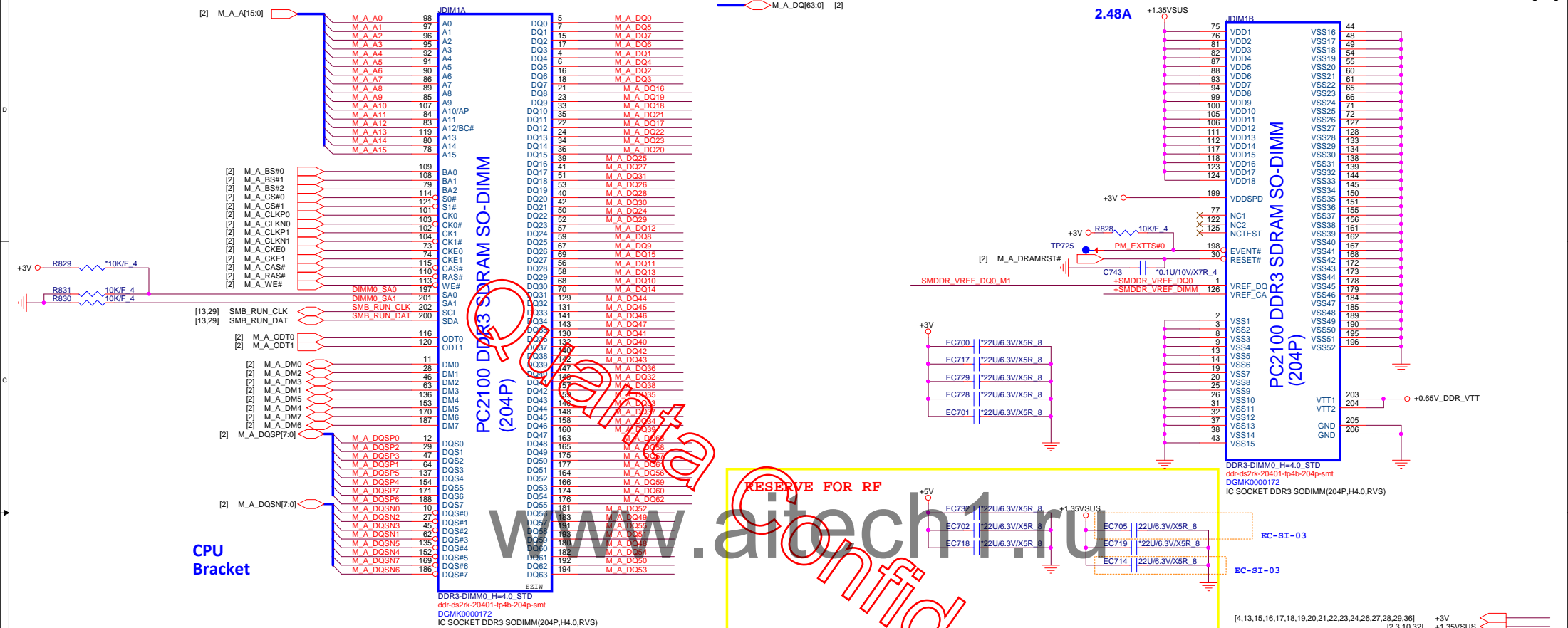
## REQUIRED STRAPS

	GPIO_SUS0	GPIO_SUS1	TOP_SWAP	GPIO_SUS3	BIOS_STRAP	SOC_Override	GPIO_SUS6	SOC_KCB_SMI	GPIO_SUS8
PULL HIGH	DDI0 detected DEFAULT	DDI1 detected DEFAULT	Normal Operation DEFAULT	Reserve 10 KΩ PU DEFAULT	SPI DEFAULT	Normal Operation	10 KΩ PU to 1.8V DEFAULT	Reserve 10 KΩ PU DEFAULT	Supply is 1.35V
PULL LOW	DDI0 not detected	DDI1 not detected	Change Boot Loader address		LPC	Override DEFAULT			Supply is 1.25V DEFAULT

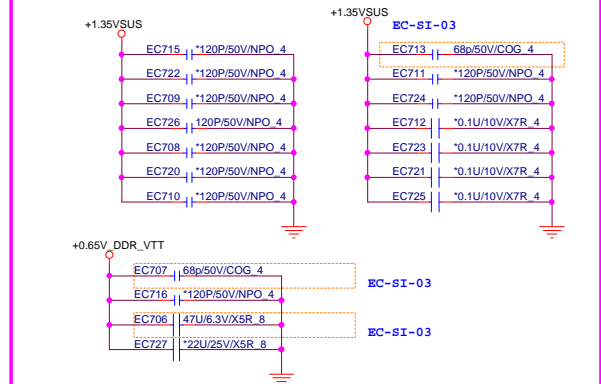
	CAM08	CAM09	CAM11
PULL HIGH	ICLK Xtal OSC Bypass	CCU SUS RO Bypass	RTC OSC Bypass
PULL LOW	ICLK Xtal OSC No Bypass DEFAULT	CCU SUS RO No Bypass DEFAULT	RTC OSC No Bypass DEFAULT

[4,5,6,7,8,10,13,28,29,33,34] +1.8VS5

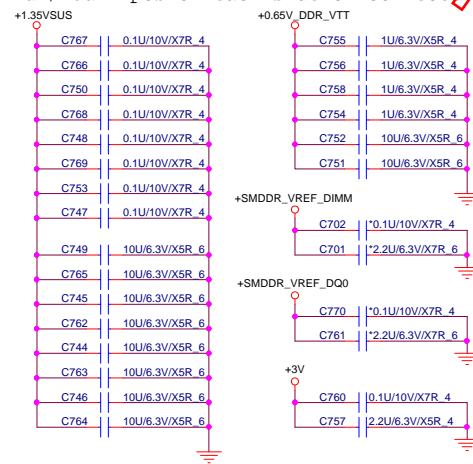




**For EMI RESERVE**

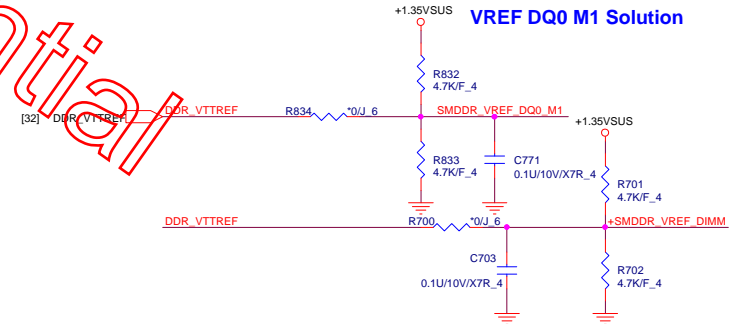


**Place these Caps near So-Dimm0.**  
F 4pcs on each side of connector



Near SO-DIMM

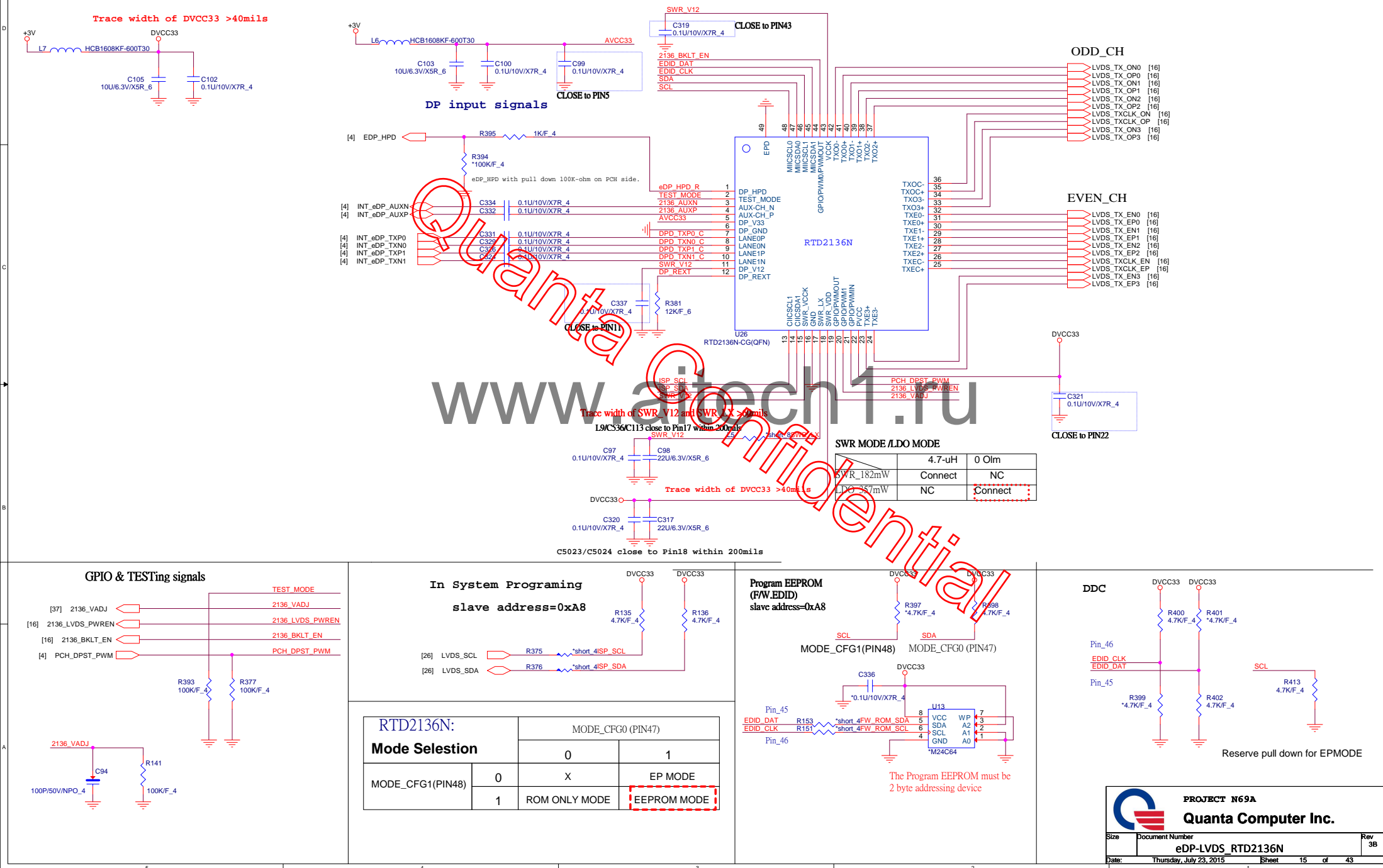
## VREF DQ0 M1 Solution



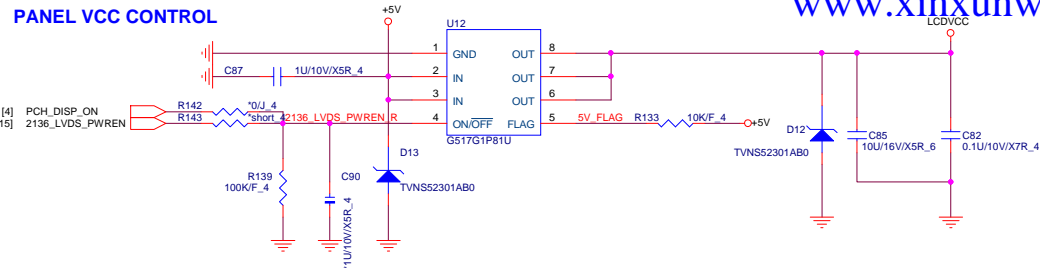
**PROJECT N69A**  
**Quanta Computer Inc.**

Size	Document Number	Re
	DDR3 DIMM0-STD(4.0H)	
Date:	Thursday, July 23, 2015	Sheet 14 of 43

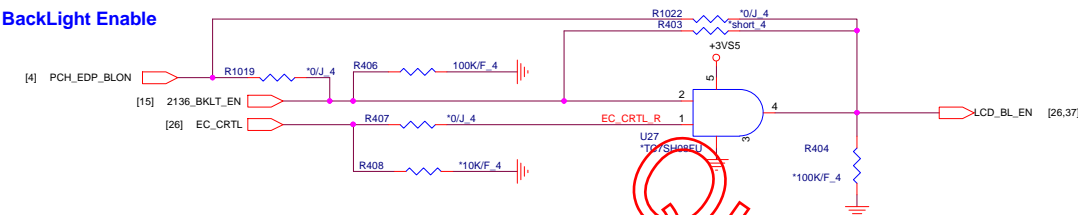
## eDP to LVDS (RTD2136N-CG)



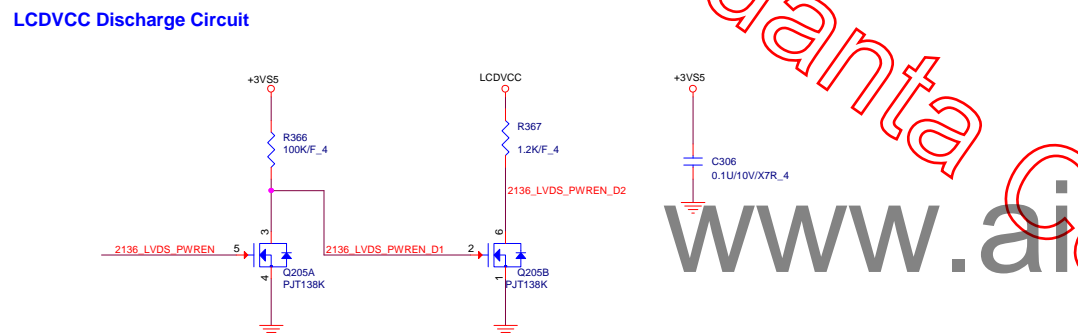
# PANEL VCC CONTROL



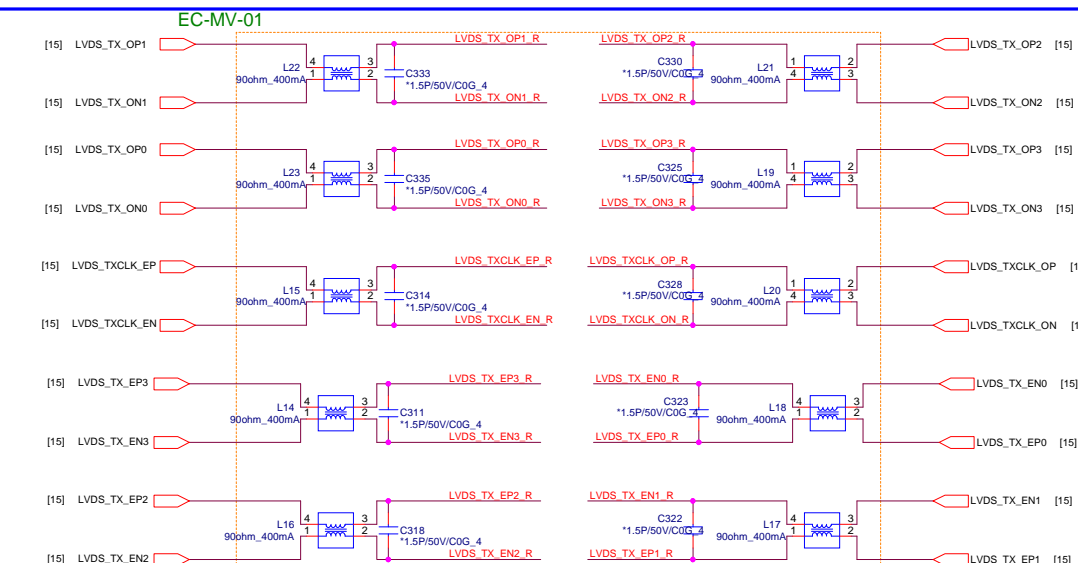
# BackLight Enable



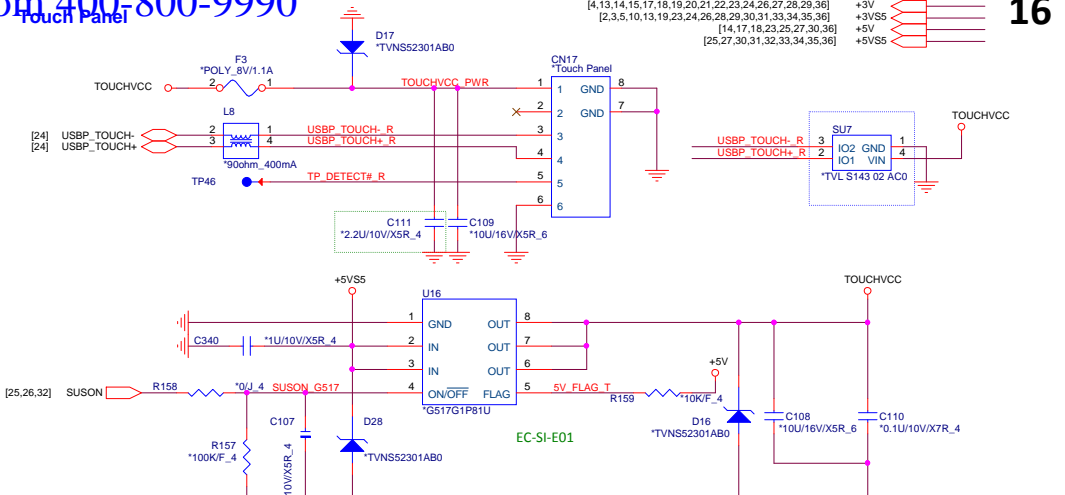
# LCDVCC Discharge Circuit



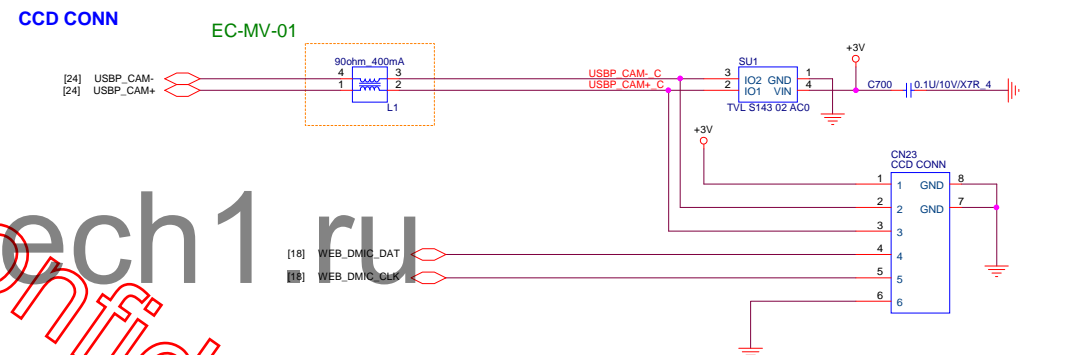
# EC-MV-01



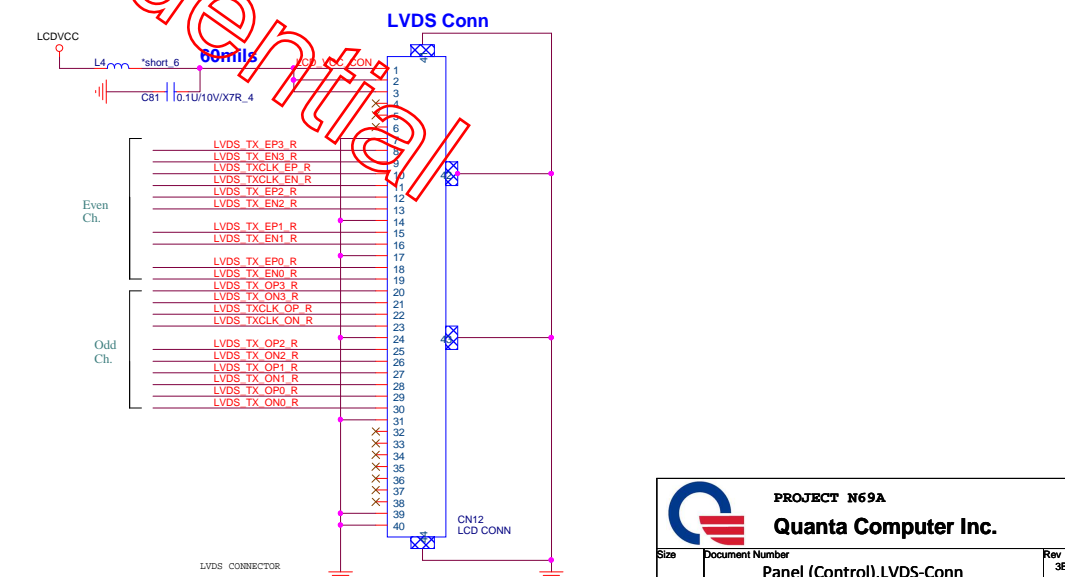
# Touch Panel

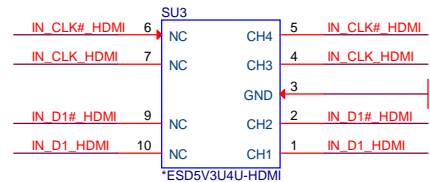
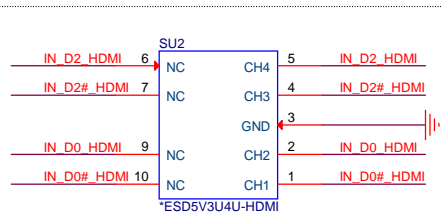
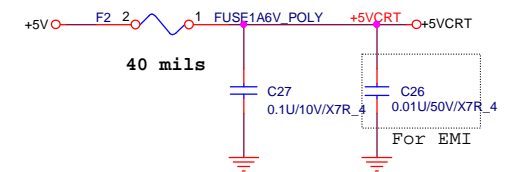
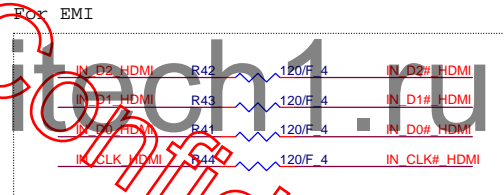
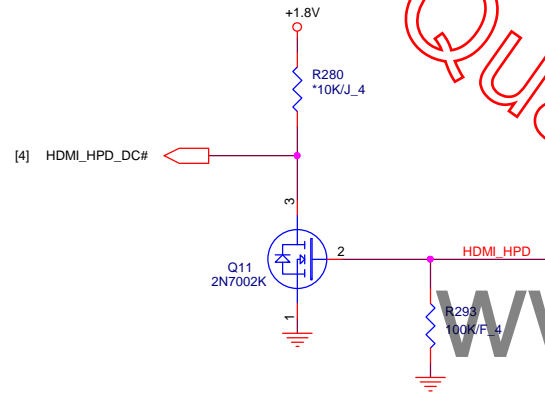
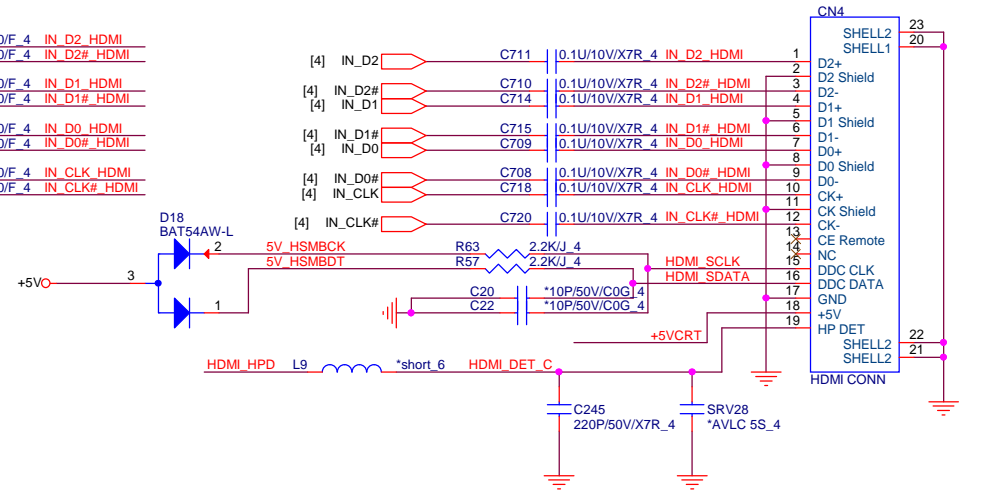
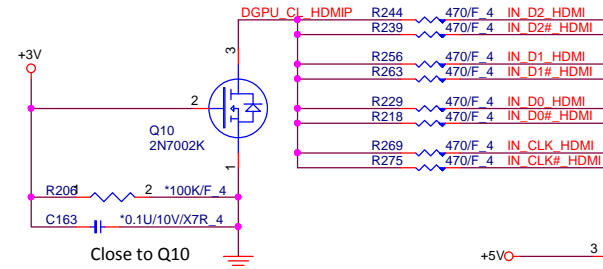
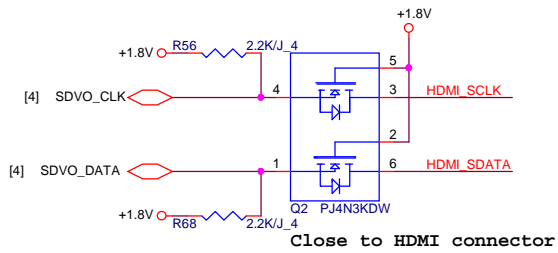


# CCD CONN

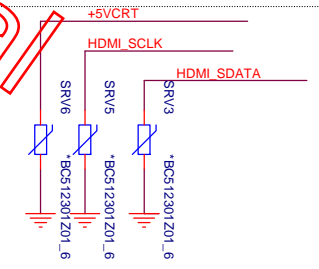


# LVDS Conn



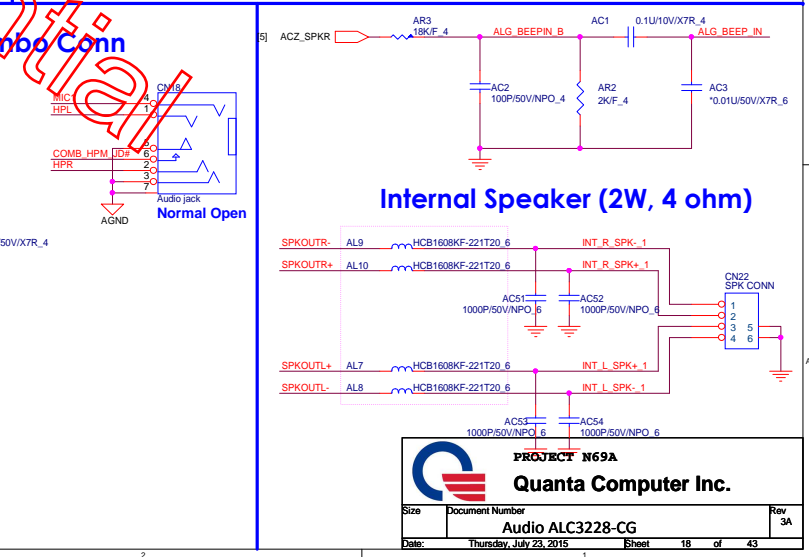
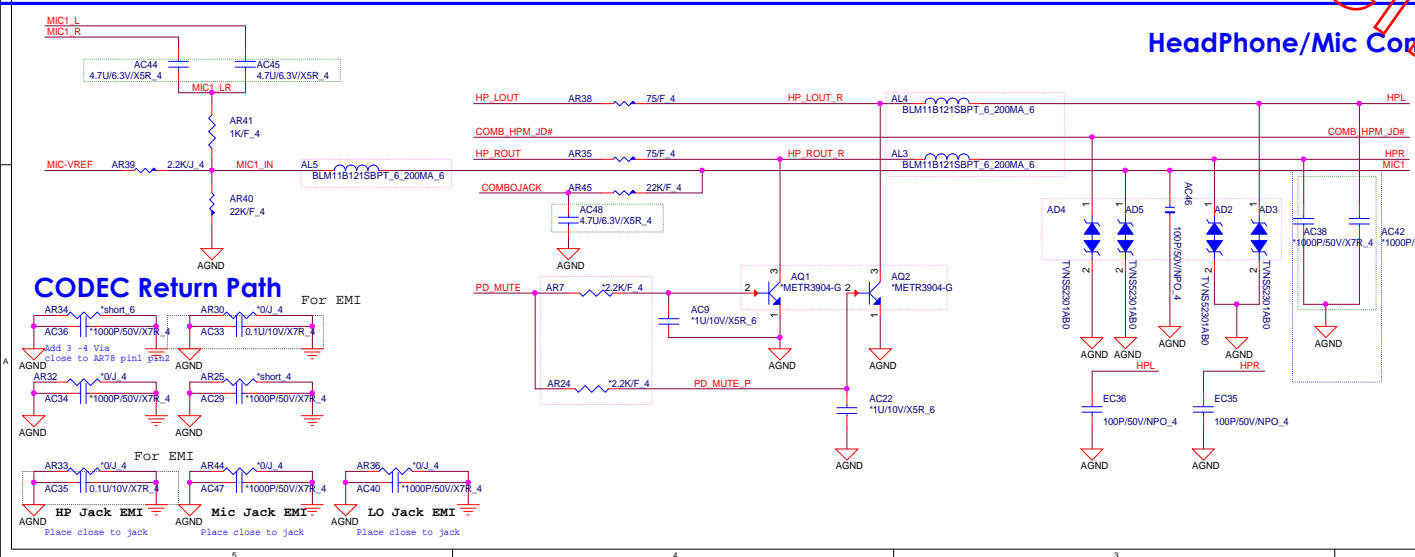
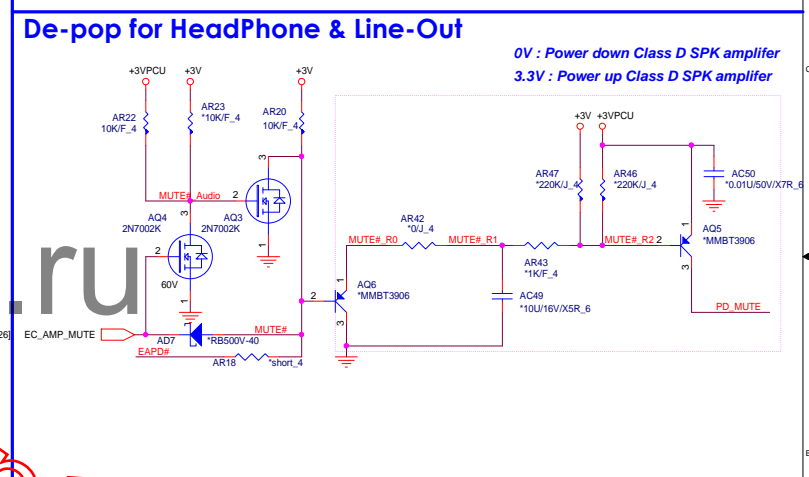
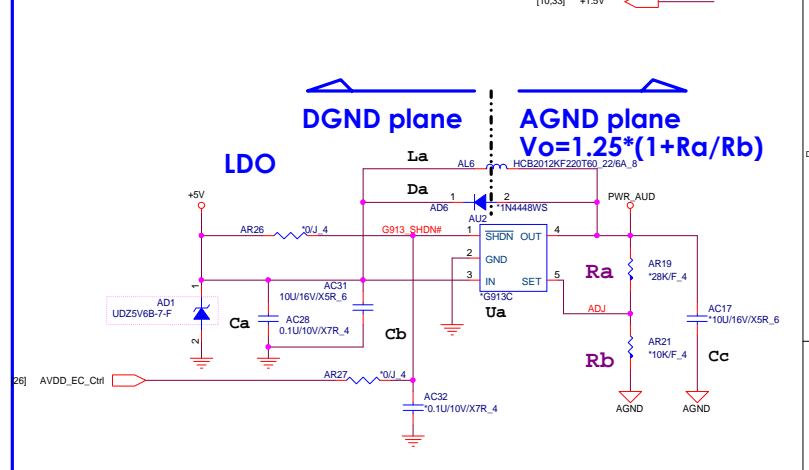
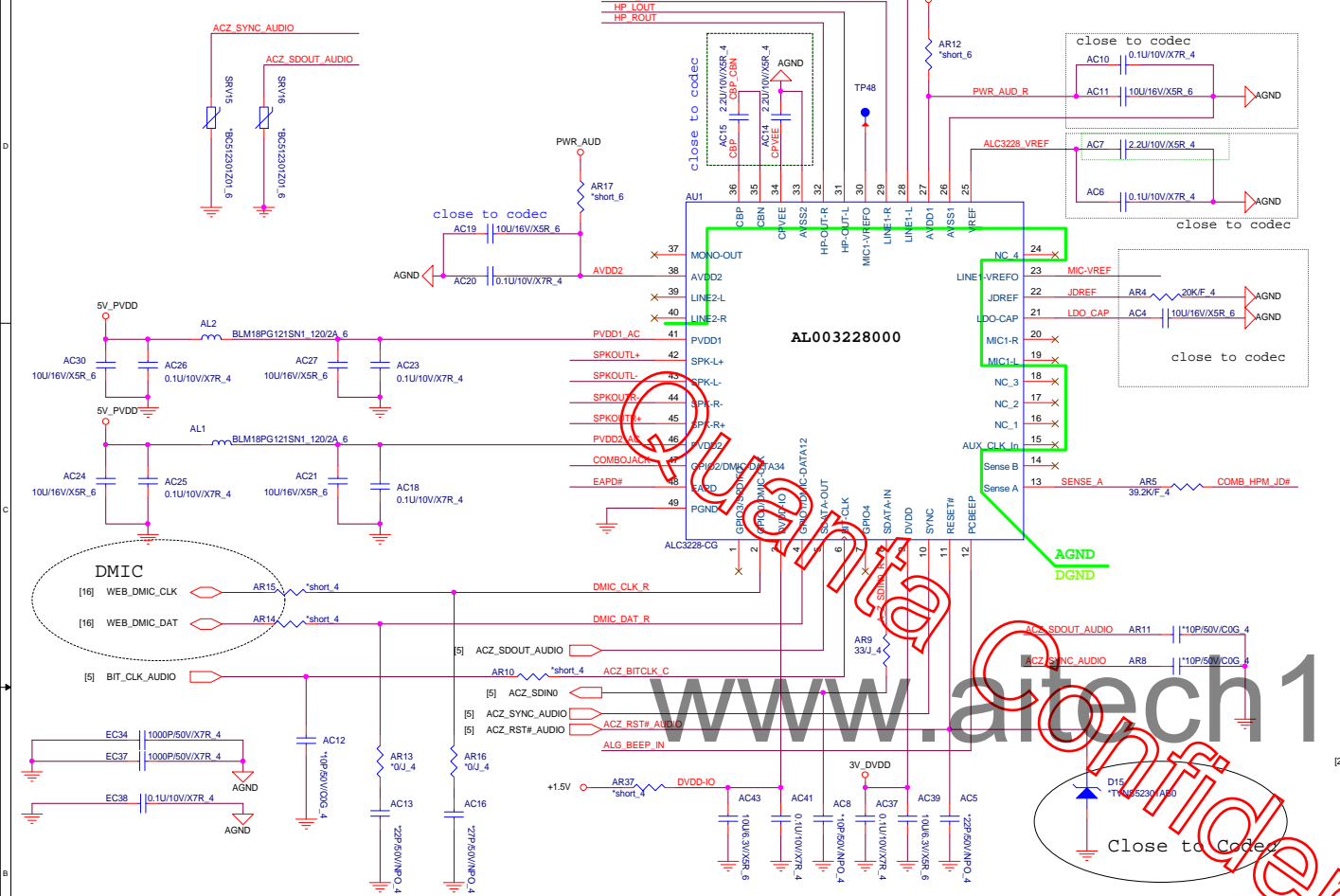


Layout note: Place close to HDMI Conn

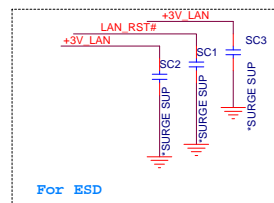


[4,5,19,22,23,27,33]  
[4,13,14,15,16,18,19,20,21,22,23,24,26,27,28,29,36]  
[14,16,18,23,25,27,30,36]

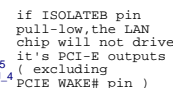
+1.8V  
+3V  
+5V



+3V  
+3VS5



For

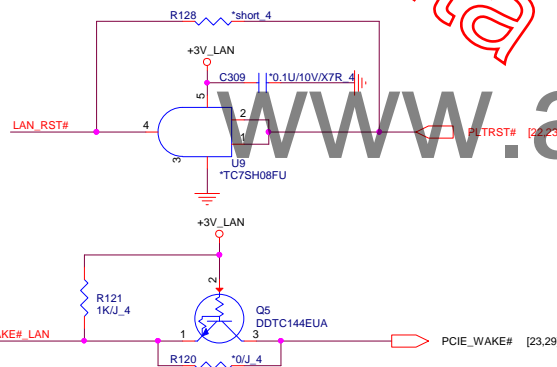


close to each VDD10 pin-- 8, 30

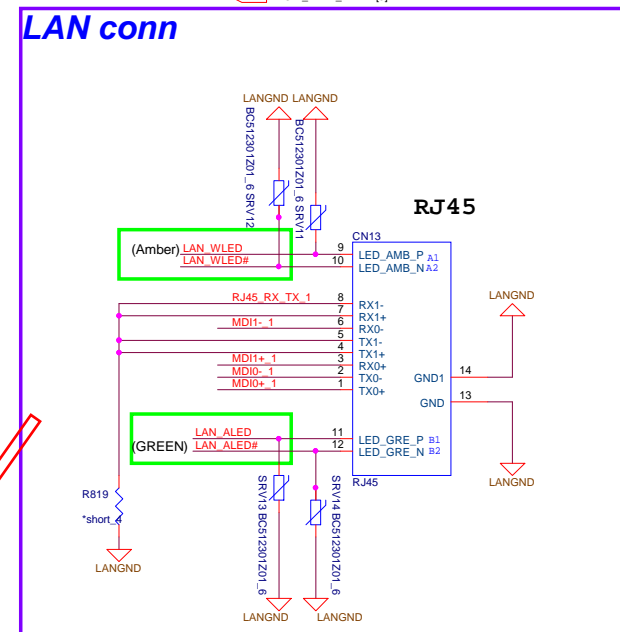
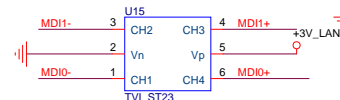
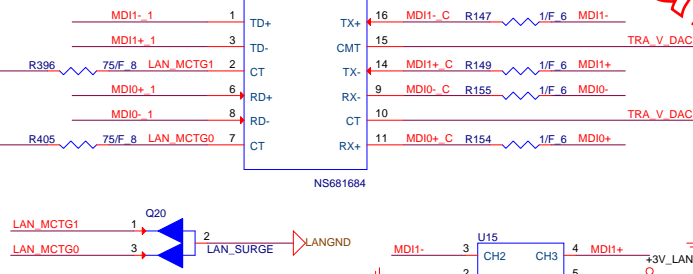
>60mil

NA: Ca, Cb  
Stuff La(0ohm), Cz

Place Cg Ch close to each VDD10 pin - 30 (reserve)



Stuff Ca and Cb only, close to each VDD33 pin-- 23, 32

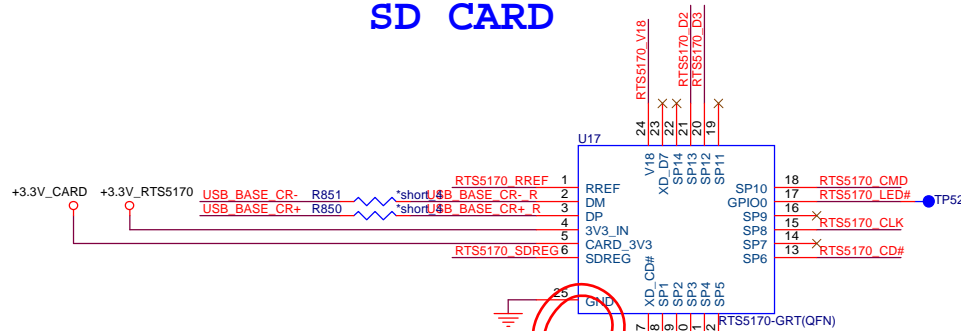


## SD/MMC CARD READER CONNECTOR (MMC)

## SD CARD

## CARD PCIE INTERFACE

## CARD POWER



EXT.SD

[24] USB\_BASE\_CR+ USB\_BASE\_CR+  
[24] USB\_BASE\_CR- USB\_BASE\_CR-

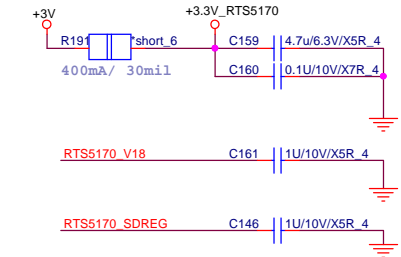
RTS5170\_CD# R176 33/J 4 SD\_CD#\_CONN  
RTS5170\_D0 R186 33/J 4 SD\_D0\_CONN  
RTS5170\_D1 R185 33/J 4 SD\_D1\_CONN  
RTS5170\_D2 R195 33/J 4 SD\_D2\_CONN  
RTS5170\_CMD R192 33/J 4 SD\_CMD\_CONN  
RTS5170\_WP R184 33/J 4 SD\_WP\_CONN

RTS5170\_D2 R194 33/J 4 SD\_D2\_CONN

C162 0.1U/10V/X7R 4  
RTS5170\_CLK R190 33/J 4 SD\_CLK\_CONN  
C147 4.7P/50V/NPO 4  
R258&C273 closed to U13

## HW STRAPS

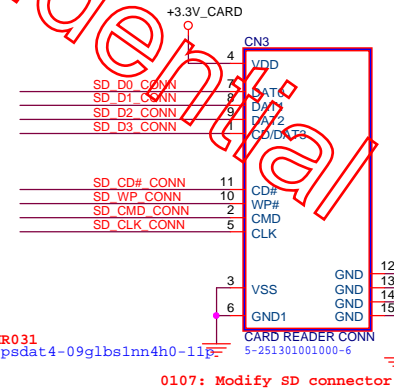
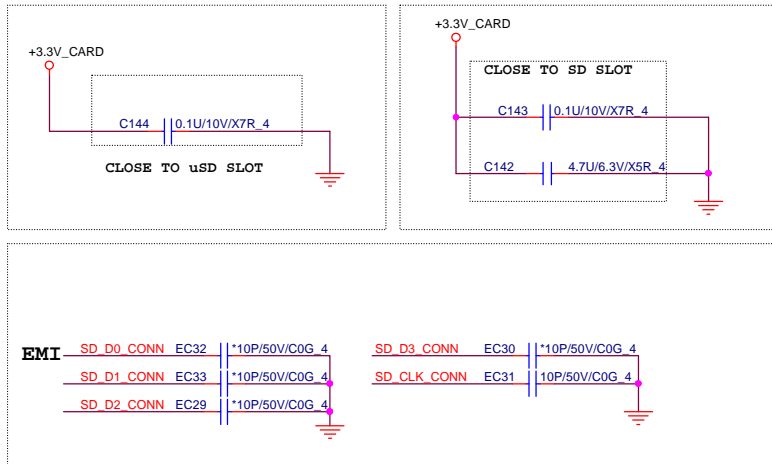
RTS5170\_RREF R193 6.2K/F 4  
CLOSE TO SD\_PIN9  
RTS5170\_WP R183 0/J 4  
0115: modify



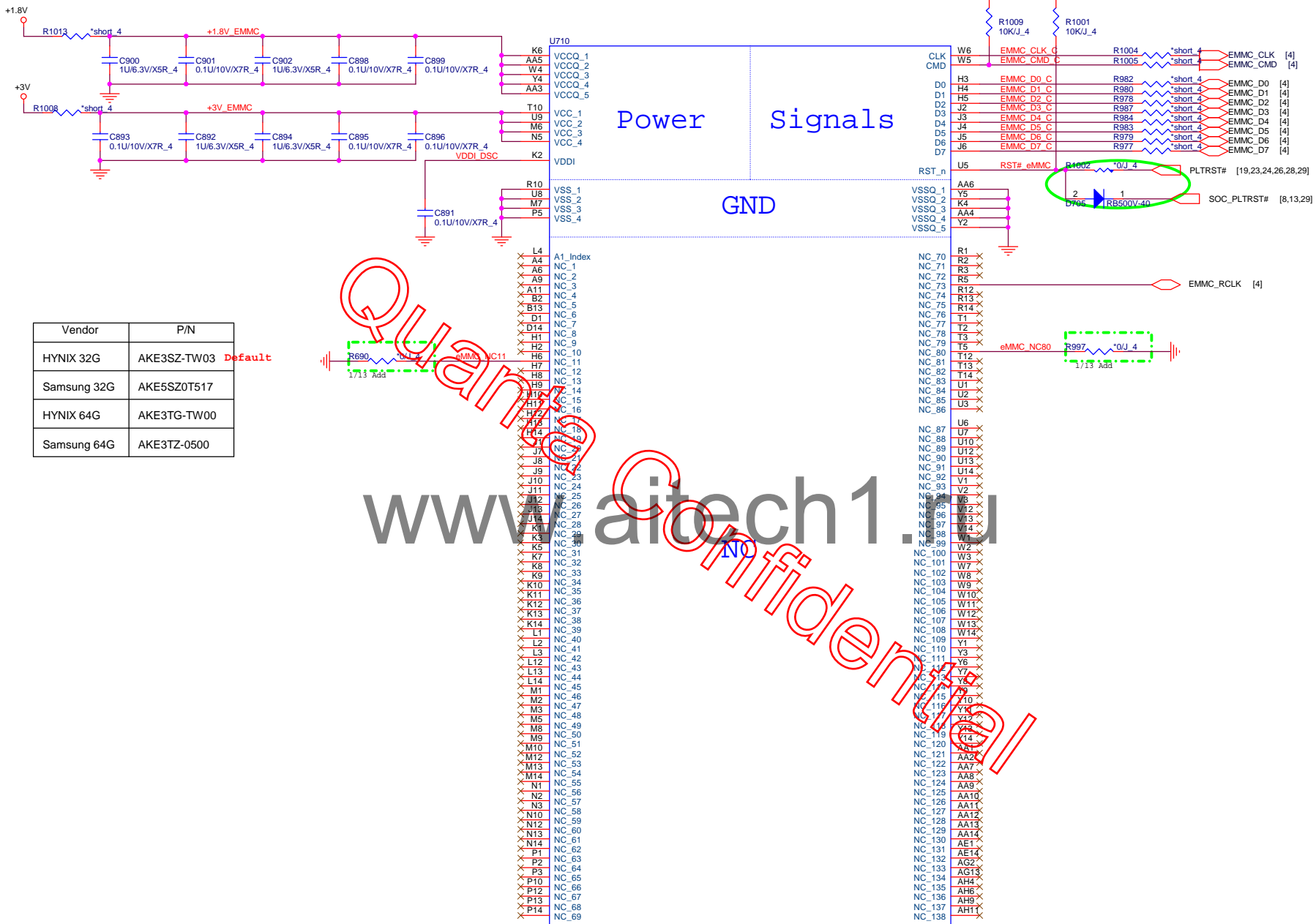
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## SD SLOT

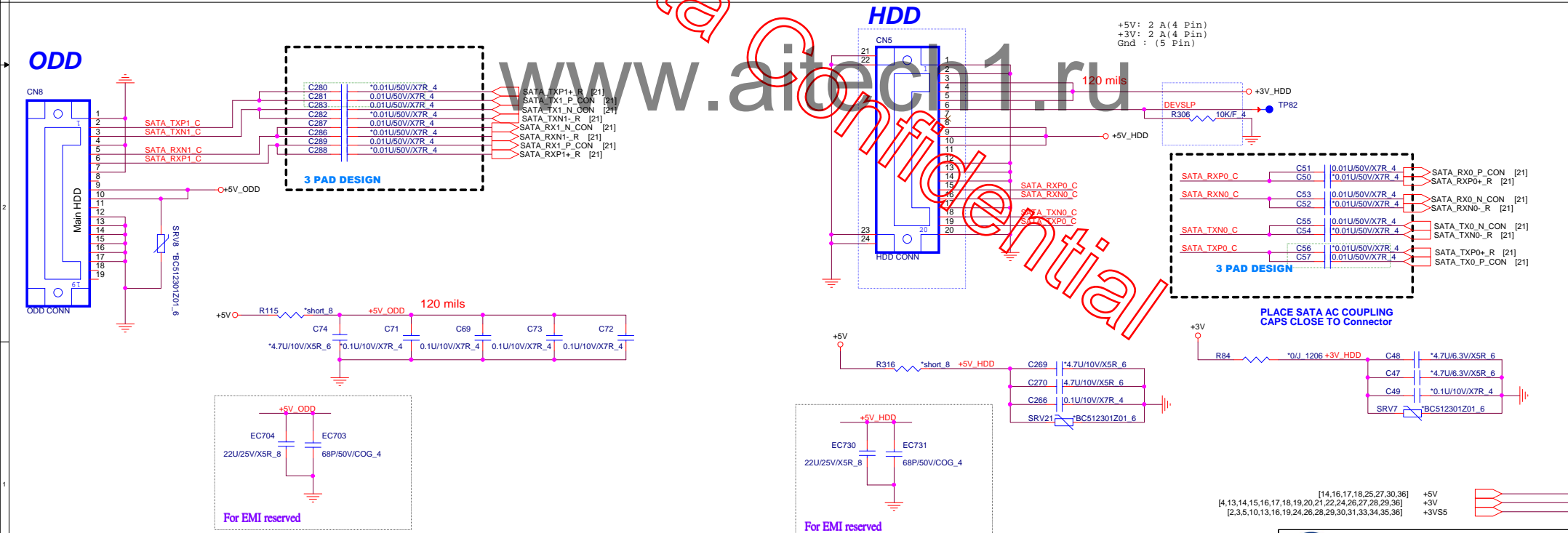
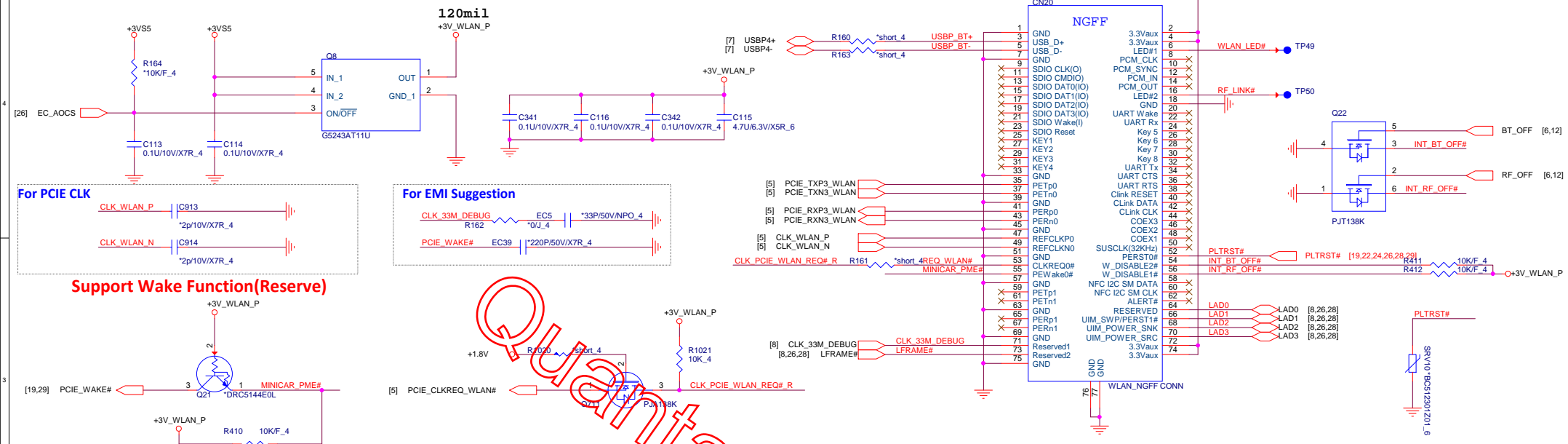
This is full size SD card

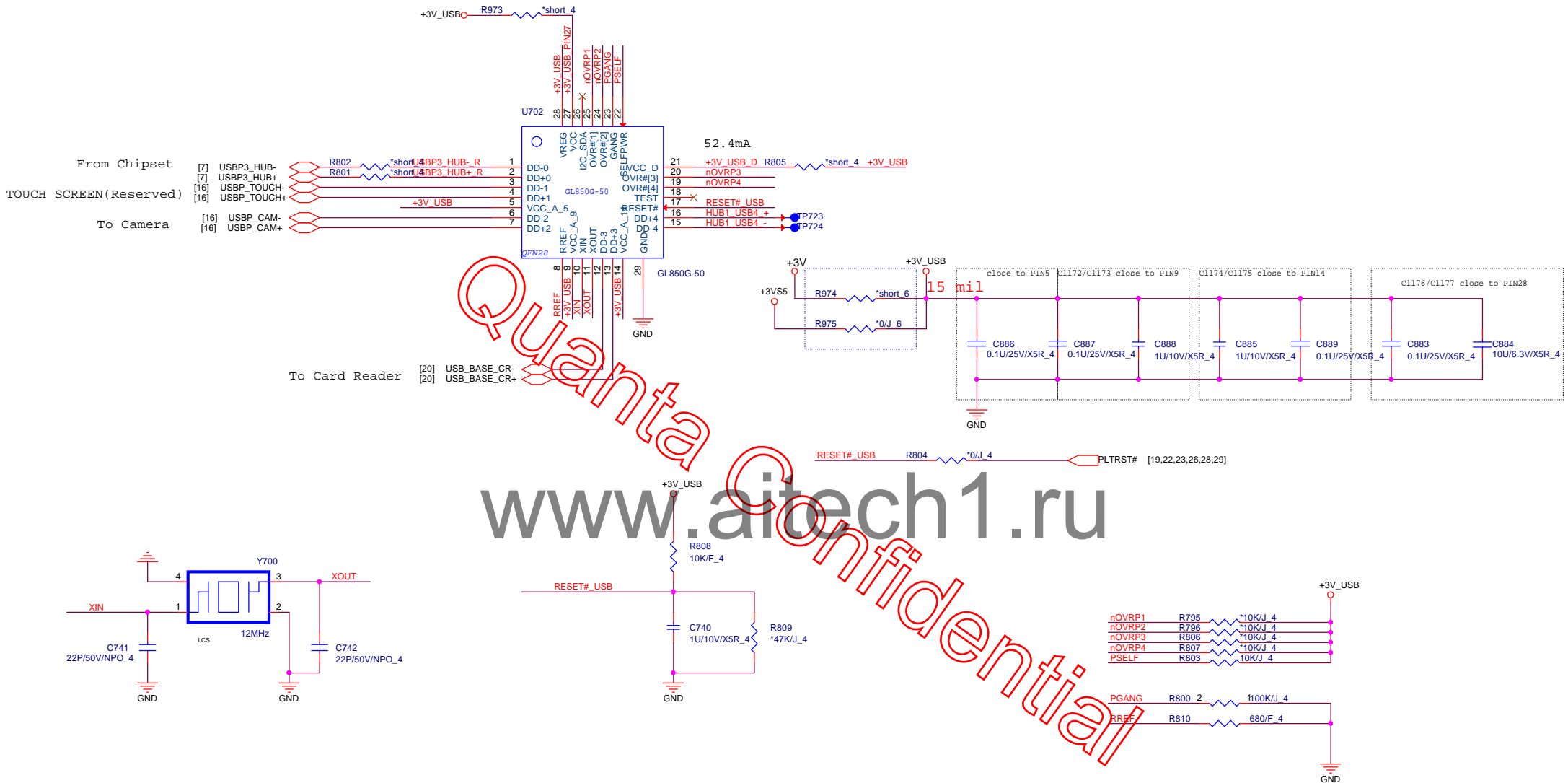


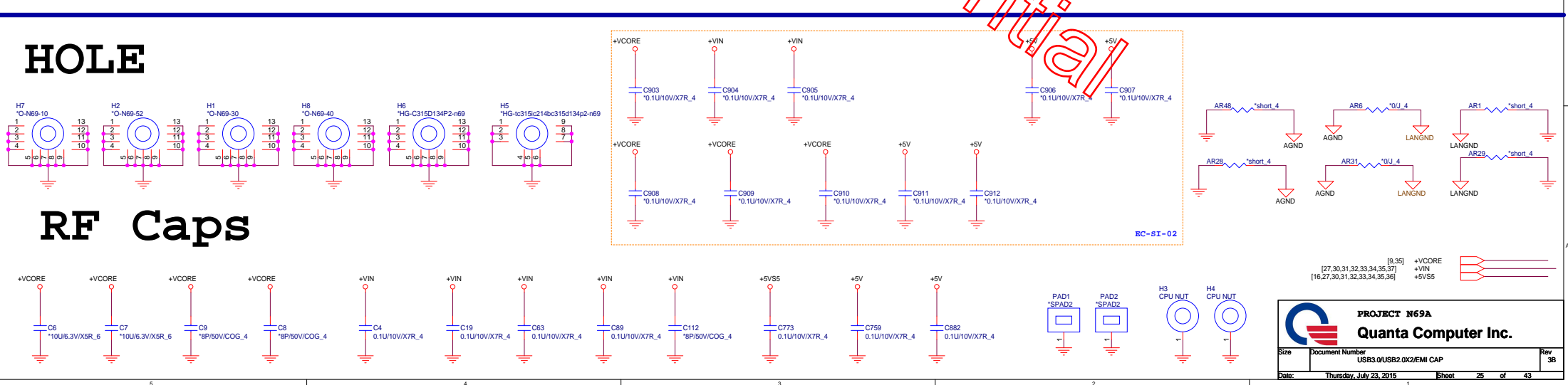
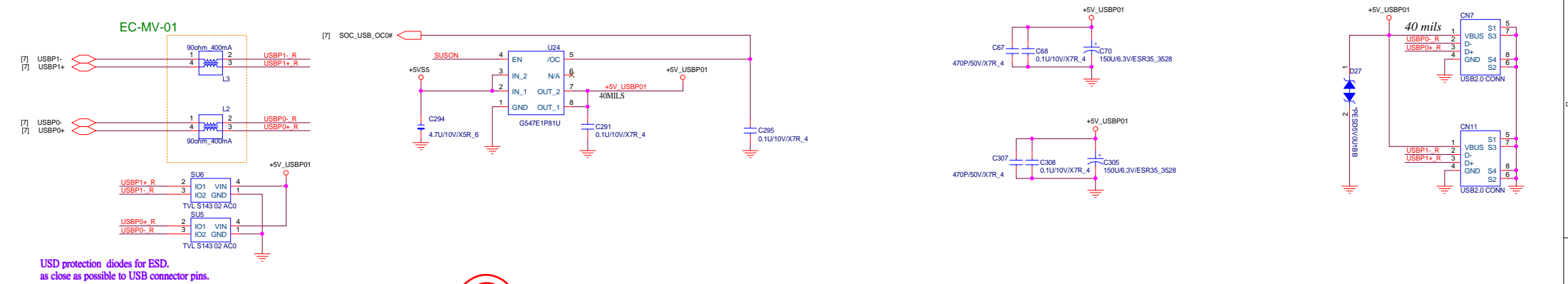


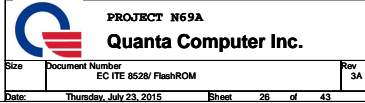


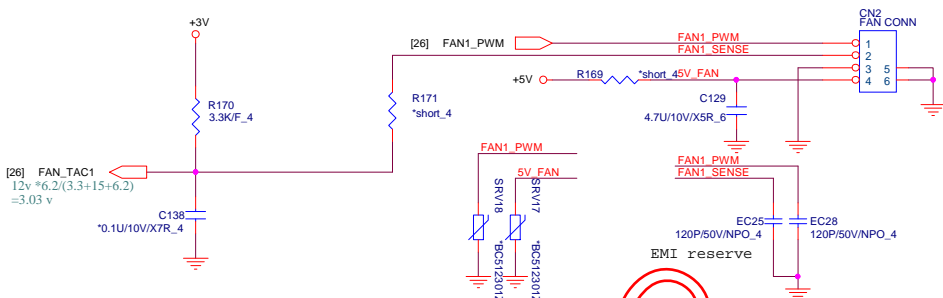
## Mini Card WLAN/BT(Optional) PCIe M.2\_power(S5)





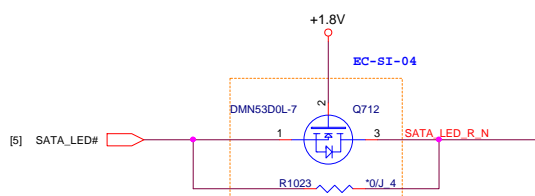
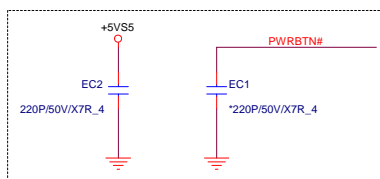
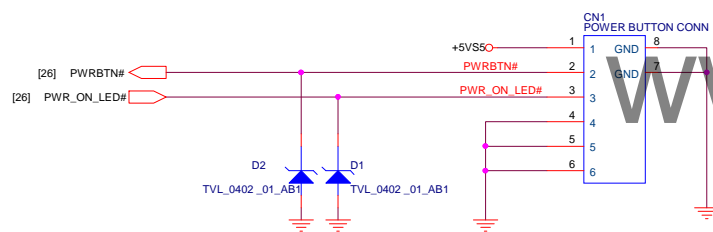




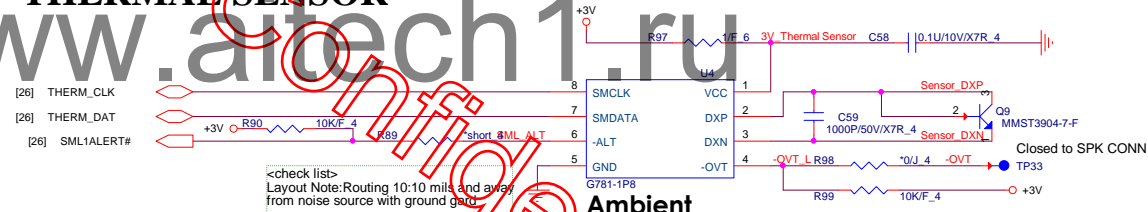


## Power Button CONN

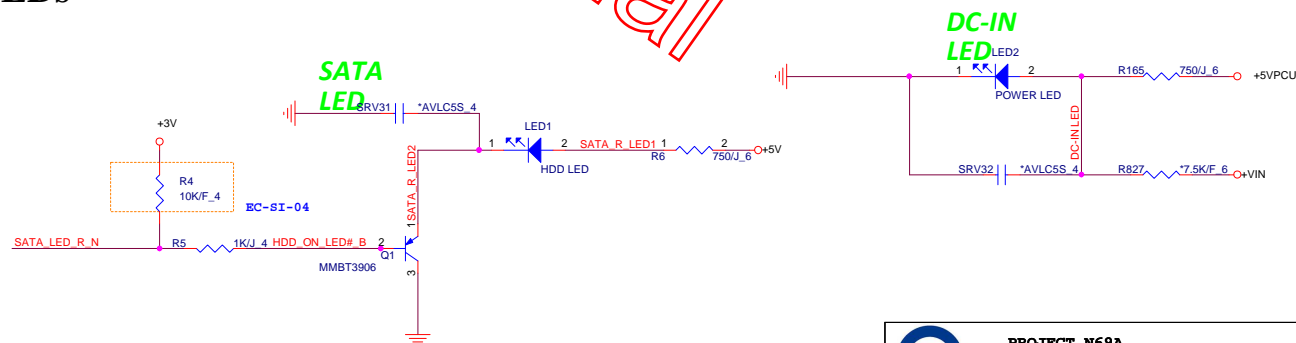
**SW1 For Debug.MP will remove it.**



# THERMAL SENSOR



## LEDs



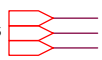
## CLR\_CMOS

Jumper	Pre-production	Production
BOOT_BLK_Recovery	X	X
BOOT_BLK_Enable	O	X

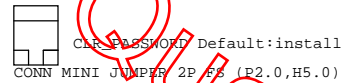
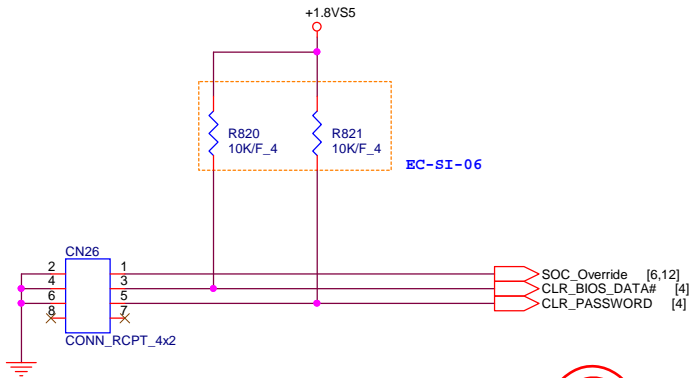
Jumper	Type
Pop	CLR_BIOS_DAT
Pop	CLR_PASSWD
Pop	BOOT_BLK_Recovery
Pop	BOOT_BLK_Enable

[2,3,5,10,13,16,19,23,24,26,29,30,31,33,34,35,36]  
[4,5,6,7,8,10,12,13,29,33,34]  
[4,13,14,15,16,17,18,19,20,21,22,23,24,26,27,29,36]

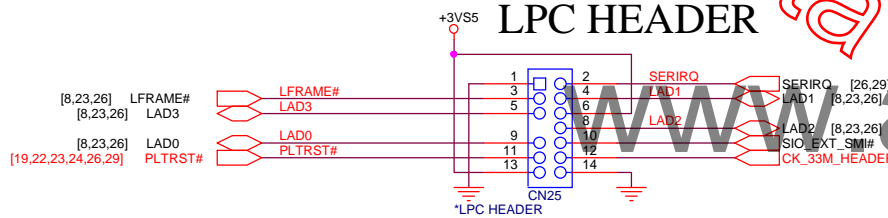
+3VS5  
+1.8VS5  
+3V



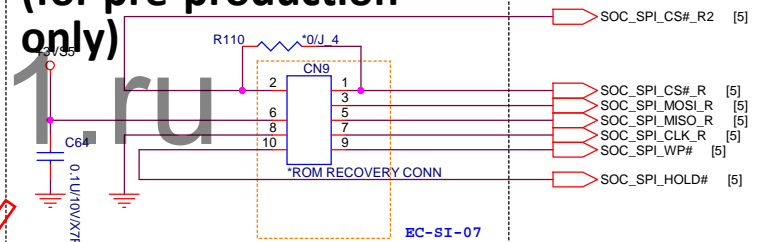
28



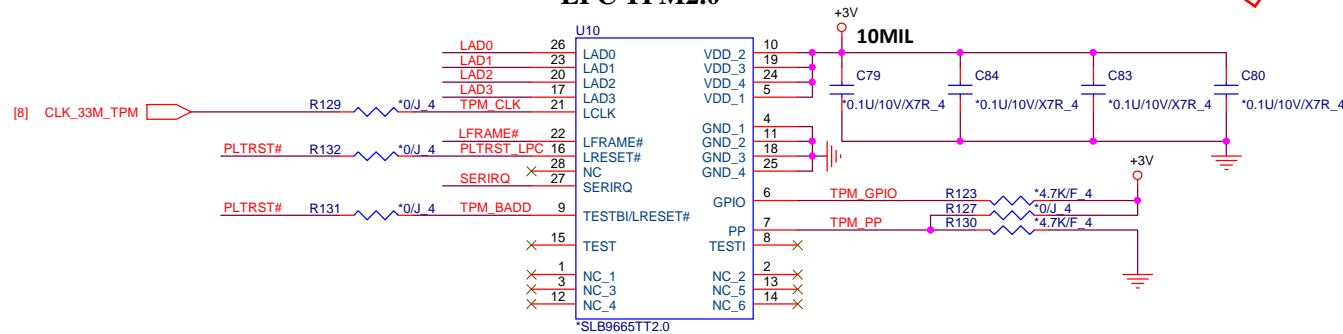
ON Chip select:Default:iinsatall (PROTO only)  
CONN MINI JUMPER 2P 5S (P2.0, H5.0)



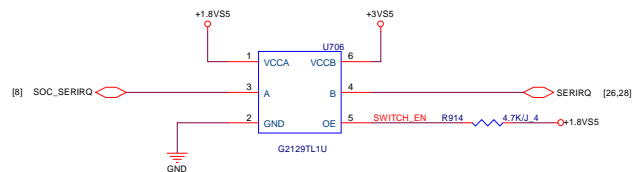
## ROM recovery (for pre-production only)



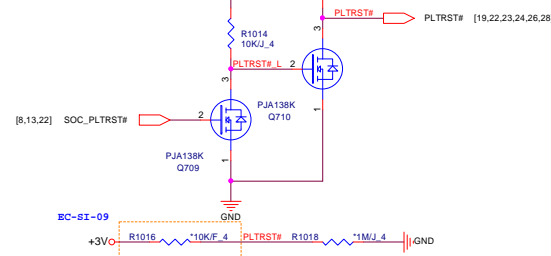
## LPC TPM2.0



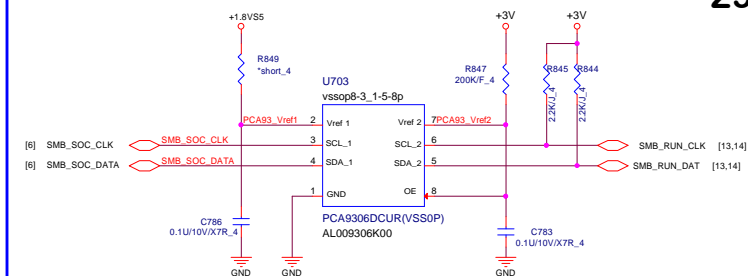
## SERIRQ



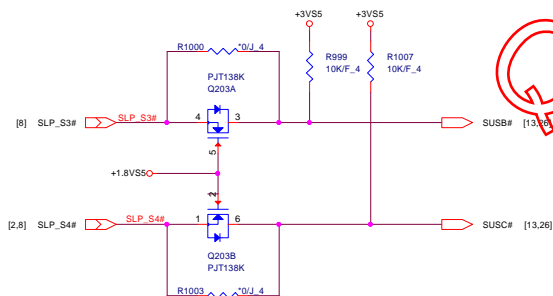
www.xinxunwei.com 400-800-9990



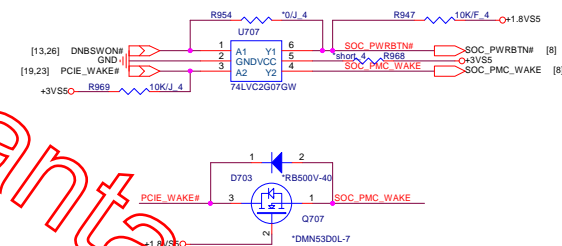
## SO-DIMM/XDP SMBUS



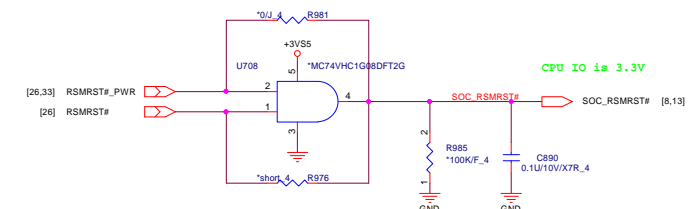
## SUSB/C#



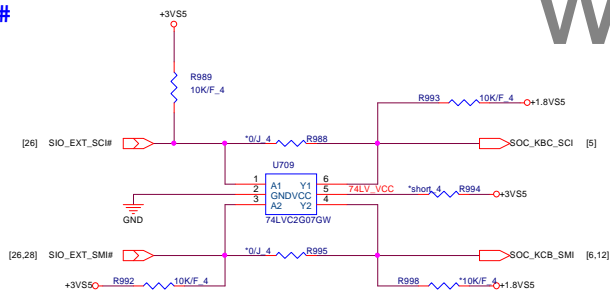
## PWRBTN#/PCIE\_WAKE#



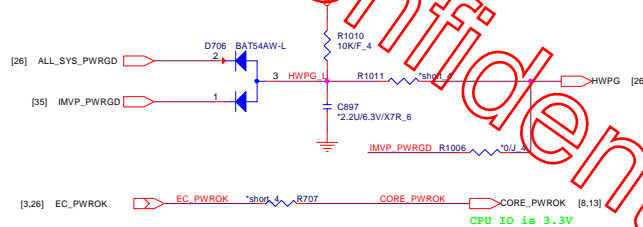
## RSMRST#



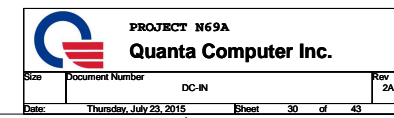
## SCI#/SMI#



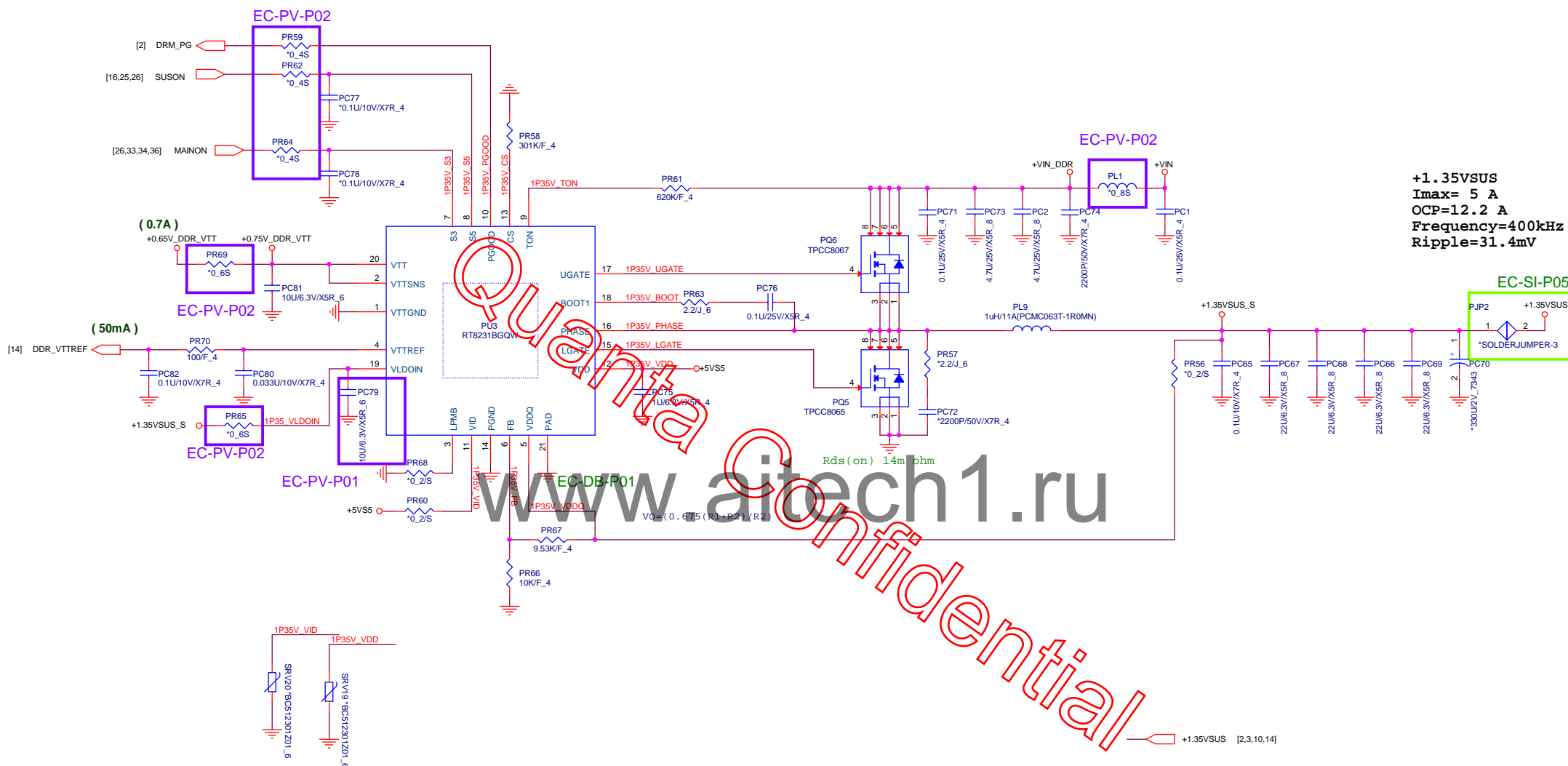
## SYS\_PWRGD

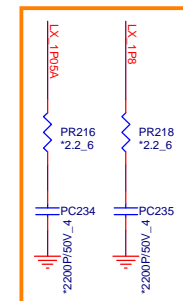


[4,13,14,15,16,17,18,19,20,21,22,23,24,26,27,28,36] +3V  
[4,5,6,7,8,10,12,13,28,33,34] +1.8VS5  
[2,3,5,10,13,16,19,23,24,26,28,30,31,33,34,35,36] +3VS5

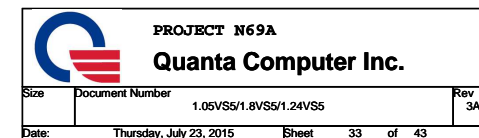


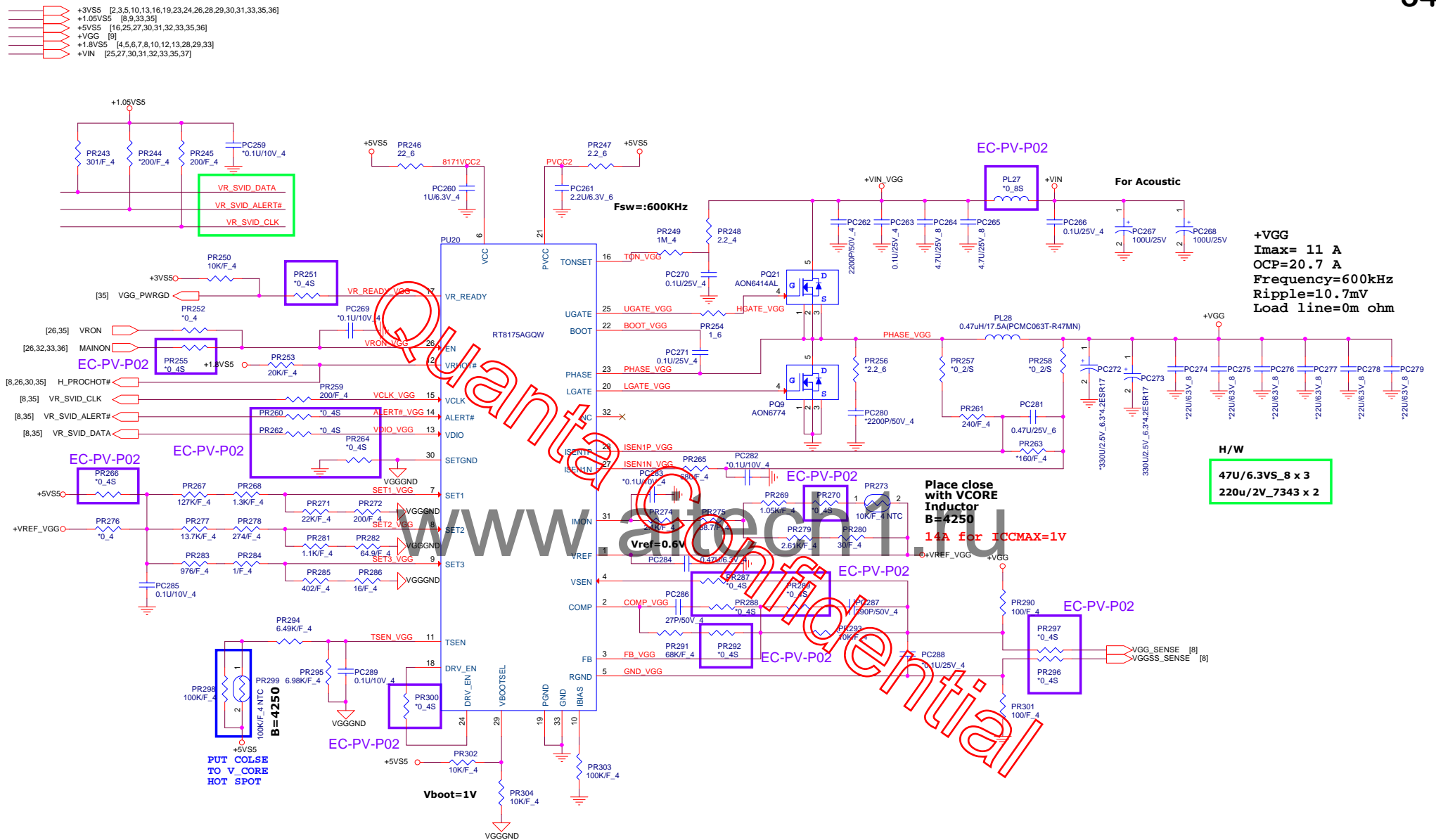


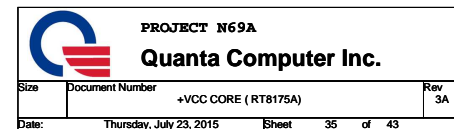


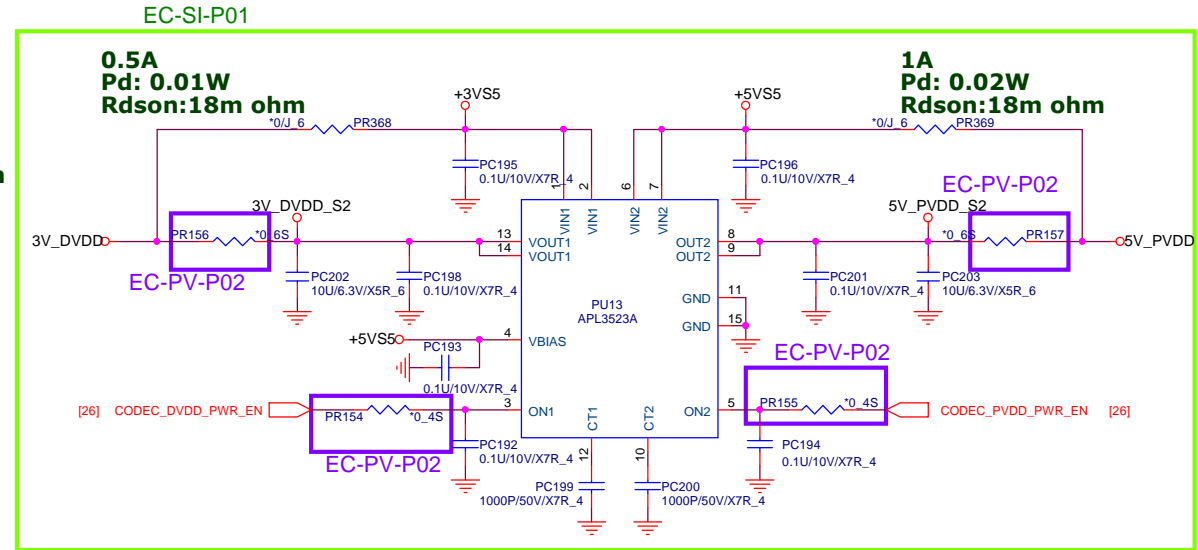
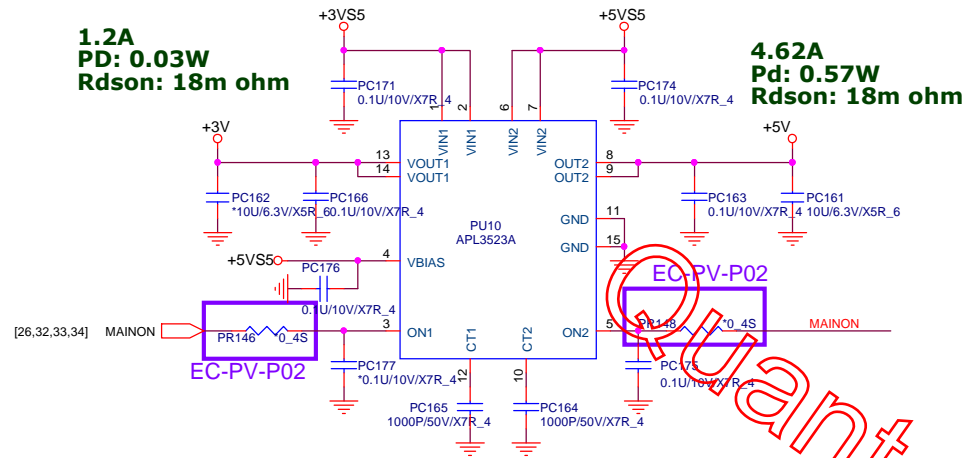


## Snubber



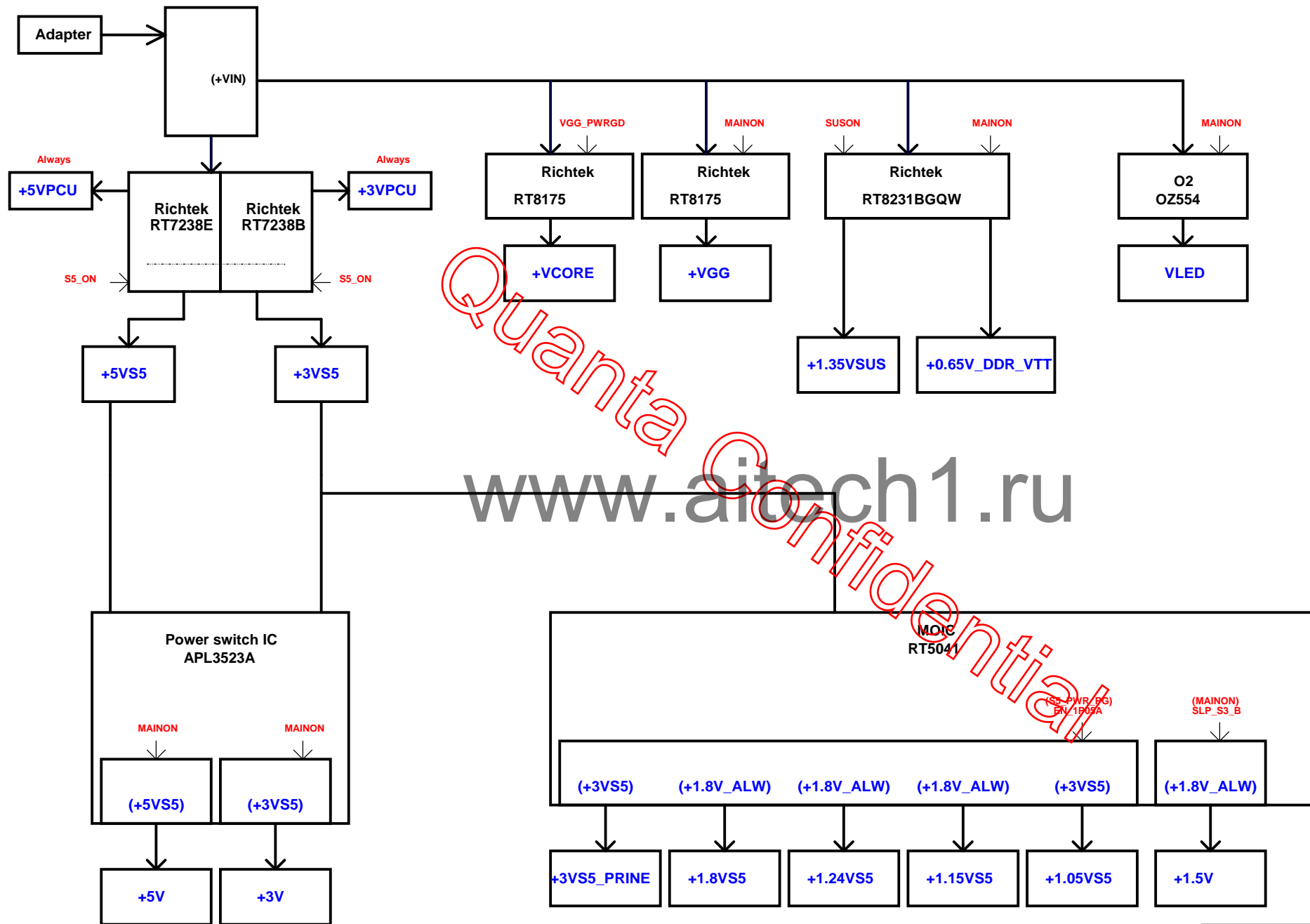


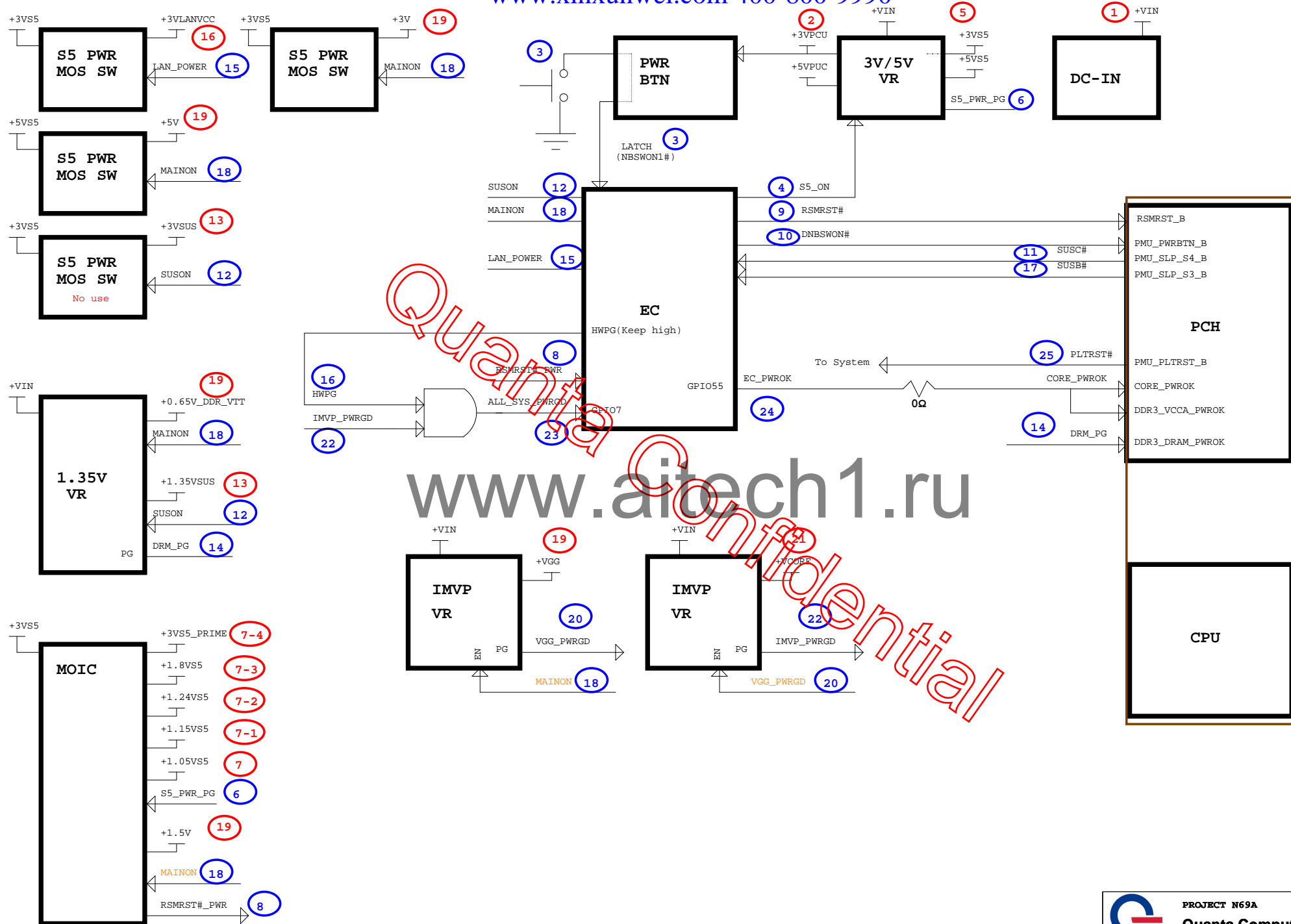


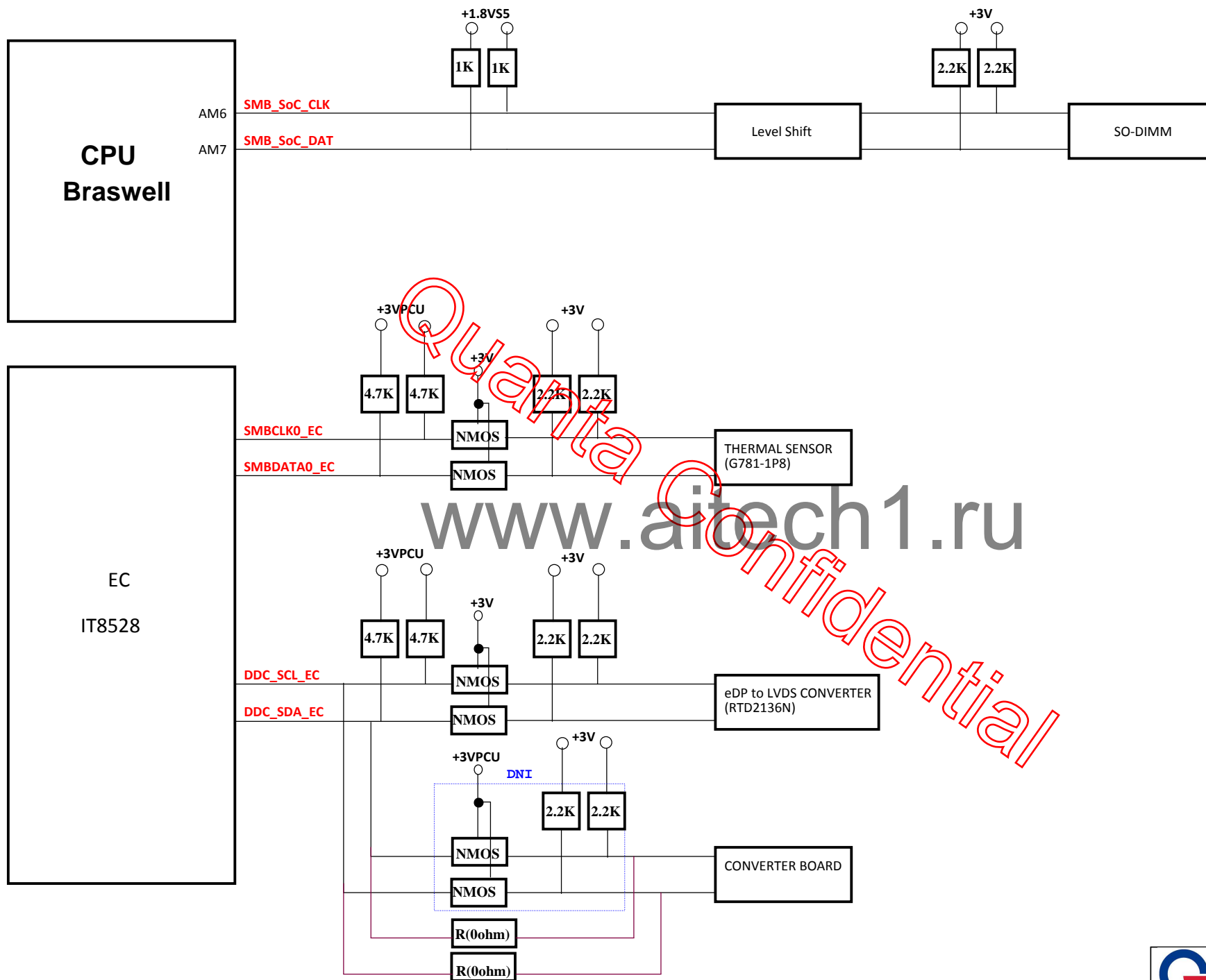


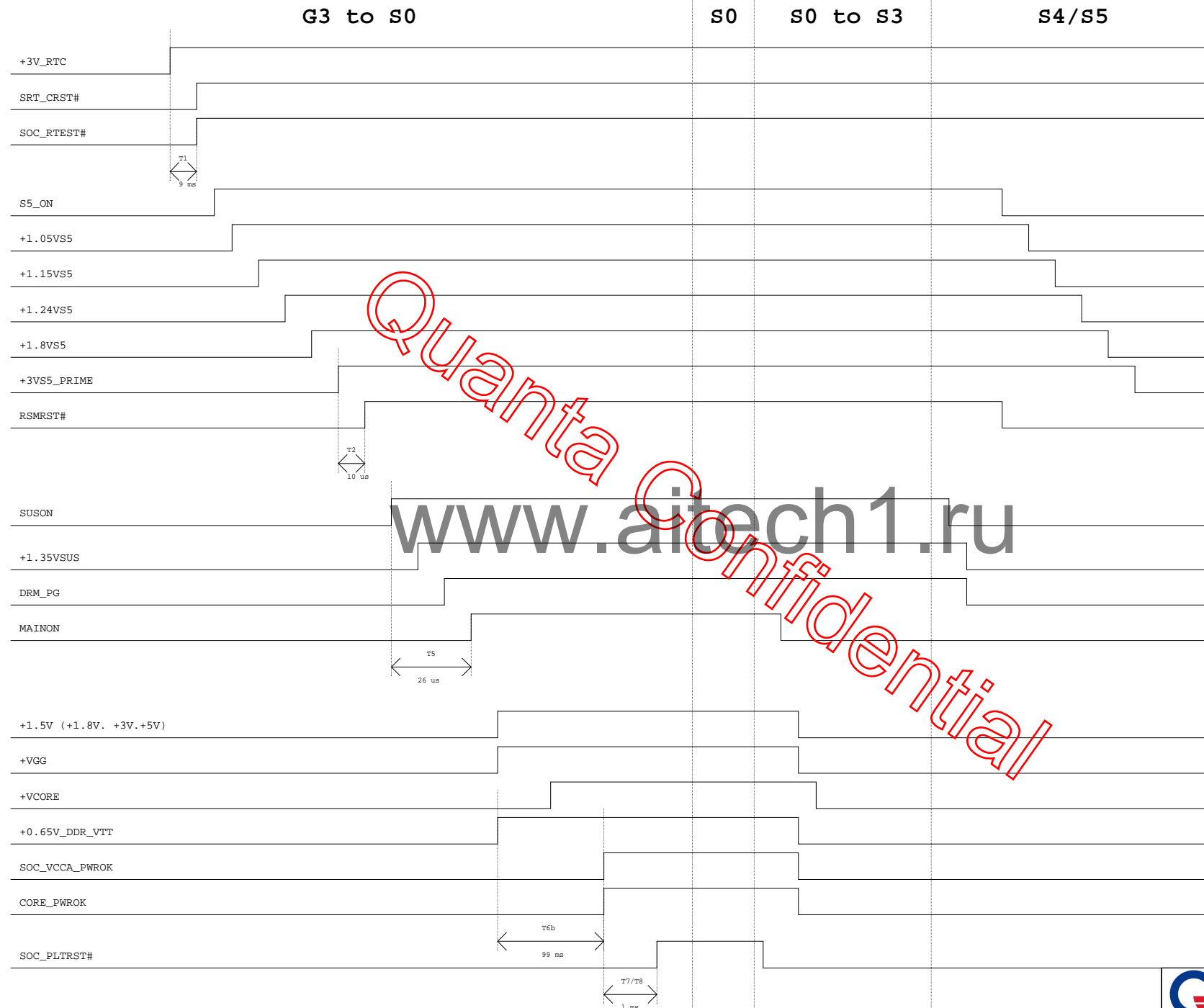
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PROJECT N69A

Quanta Computer Inc.

N69A EE Schematic EC Tracking Record DB to SI version

EC #	Page	Description	Part Affected
EC-SI-01	13	XDP reserve	C744,C775,C776,C779,CN701,R836,R837,R838,R839,R840,R841,R843
EC-SI-02	25	ESD Reserve	C903,C904,C905,C906,C907,C908,C909,C910
EC-SI-03	14	RF request	EC705,EC706,EC707,EC713,EC714
EC-SI-04	27	SATA LED ALWAYS light issue	add Q712,R4,un-stuff R1023
EC-SI-05	06	Board ID change to SI	R721 un-stuff, R722 stuff
EC-SI-06	28	CLR_BIOS_DATA#/CLR_PASSWORD function	R820,R821 stuff
EC-SI-07	28	ROM recovery connector remove	CN9
EC-SI-08	21	SATA redriver IC remove	U19,U21
EC-SI-09	21,06,29,26	S5 leakage current	R797,R733,R734,R1016,R357,R358

N69A EE Schematic EC Tracking Record SI to PV version

EC-PV-01	2,4,7,8,9,10,12,15,16,17,18,19,20,21,22,23,24,25,26,29	Change 0 ohm to short pad	AR1,AR10,AR12,AR14,AR15,AR17,AR18,AR25,AR28,AR29,AR31,AR34,AR48,L4,L5,L9,R1004,R1005,R1008,R1011,R1013,R1015,R1020,R115,R128,R134,R140,R143,R150,R156,R160,R161,R163,R169,R171,R191,R213,R214,R215,R216,R227,R302,R303,R304,R305,R307,R316,R325,R326,R331,R334,R340,R341,R351,R354,R355,R375,R376,R403,R409,R703,R707,R716,R719,R723,R737,R742,R749,R764,R766,R772,R777,R782,R787,R793,R801,R802,R805,R812,R813,R815,R818,R819,R846,R848,R849,R850,R851,R853,R884,R885,R886,R89,R894,R899,R902,R913,R917,R919,R920,R922,R924,R925,R927,R928,R936,R937,R939,R940,R941,R945,R946,R953,R956,R957,R961,R968,R973,R974,R976,R977,R979,R980,R982,R983,R984,R987,R997,R994,R996
EC-PV-01	06	Board ID change to PV	R721 stuff, R722 un-stuff and R725 stuff, R726 un-stuff
EC-PV-02	16	BackLight Enable	R403 change back to 0 ohm
EC-PV-03	23	BT chock use short pad	L27 remove

N69A EE Schematic EC Tracking Record PV to MV version

EC-MV-01	16,25	Change 0 ohm to short pad	R1,R2,R108,R109,R122,R124,R308,R311,R389,R390,R391,392,R368,R369,R370,R371,R372,R374,R378,R379,R380,R382,R383,R384,R385,R386,387,R388
EC-MV-02	06	Board ID change to MV	R722 stuff, R721 un-stuff
EC-MV-03	25	USB 3.0 choke	Add L25,L26; remove R86,R87,R95,R96
EC-MV-04	15	EDID ROM	Remove U13, C336

**N69A Power Schematic EC Tracking Record DB to SI version**

EC #	Page	Description	Part Affected
EC-SI-P01	30	Change PR175, PR196, PR205, PR206 for fine tune CPU throttling function	PR175, PR196, PR205, PR206
EC-SI-P02	30	Delete reserved components	PC204,PC205,PC212,PD5,PR158,PR161,PR162,PR163,PR164,PR174, PR180,PR181,PR182,PU14
EC-SI-P03	30	Add resistors for Adaptor ID pin detect function	PR370, PR371,PR372, PR373,PR374
EC-SI-P04	31~33, 37	Change default open to default short	PJP1,PJP2,PJP7,PJP8,PJP9,PJP10

**N69A Power Schematic EC Tracking Record PV to MV version**

EC #	Page	Description	Part Affected
EC-PV-P01	32	Add PC79 as 10U/6.3V/X5R_6 for VTT transient	PC79
EC-PV-P02	31~36	Change 0 ohm to short pad	0805 PL21,PL22,PL1,PL23,PL25,PL27,PL29 0603 PR32,PR39,PR65,PR69,PR213,PR214,PR215,PR217,PR219,PR224,PR221,PR222, PR225,PR226,PR156,PR157 0402 PR175,PR177,PR367,PR179,PR189,PR199,PR200,PR208,PR211,PR373,PR374,PR29 PR31,PR36,PR59,PR62,PR64,PR223,PR230,PR231,PR232,PR233,PR242,PR251 PR255,PR260,PR262,PR264,PR266,PR270,PR287,PR288,PR289,PR292,PR296,PR297 PR300,PR315,PR319,PR320,PR322,PR324,PR326,PR328,PR329,PR332,PR349,PR351 PR352,PR355,PR357,PR359,PR362,PR146,PR148,PR154,PR155